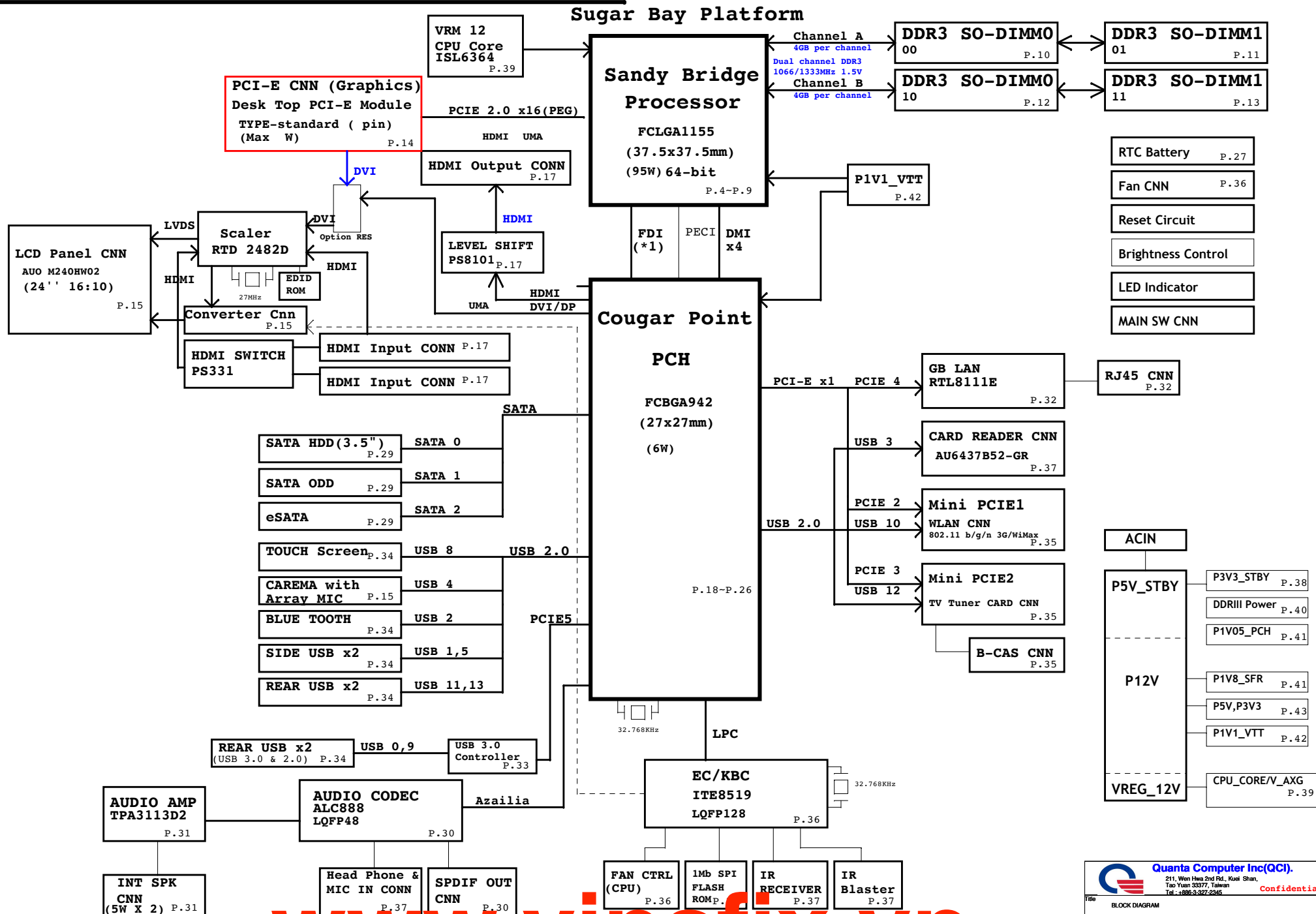


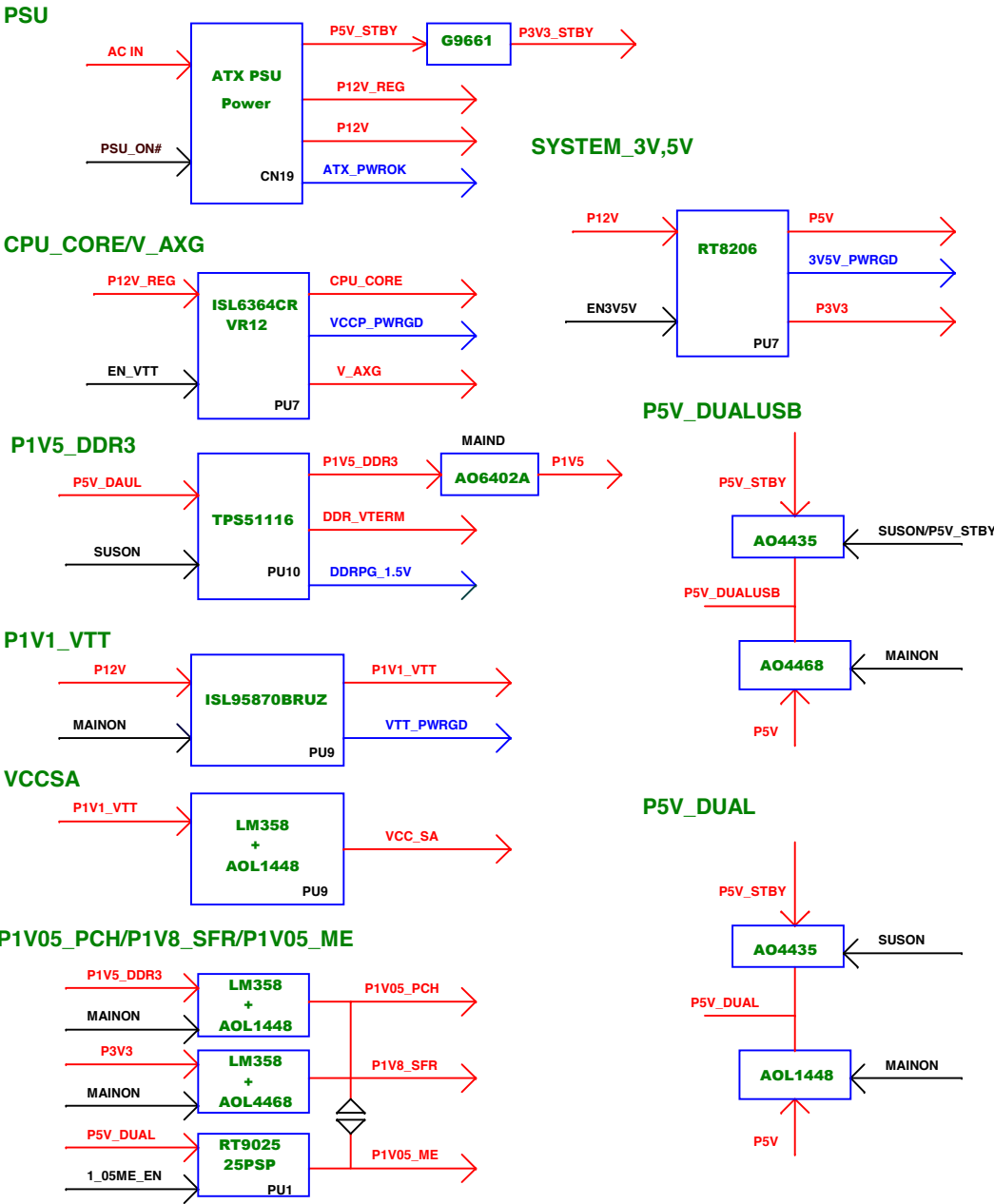
QK1 24" AIO Block Diagram :

1

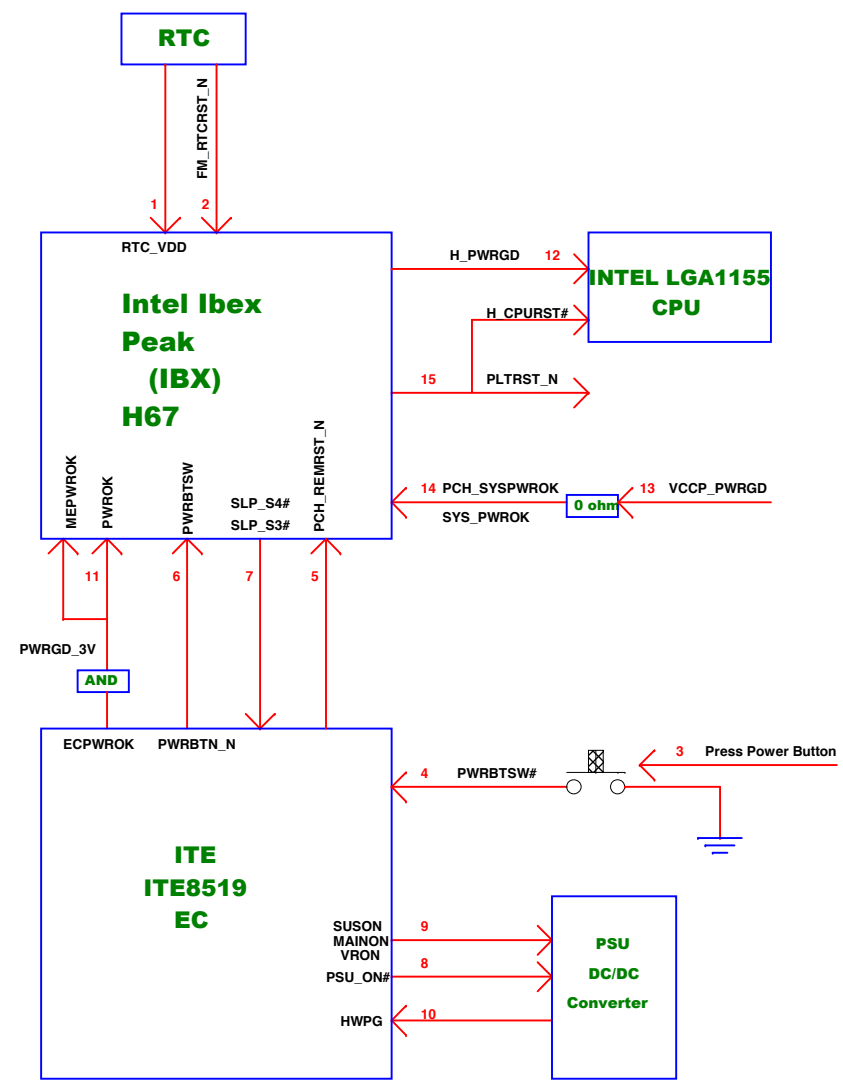


www.vinafix.vn

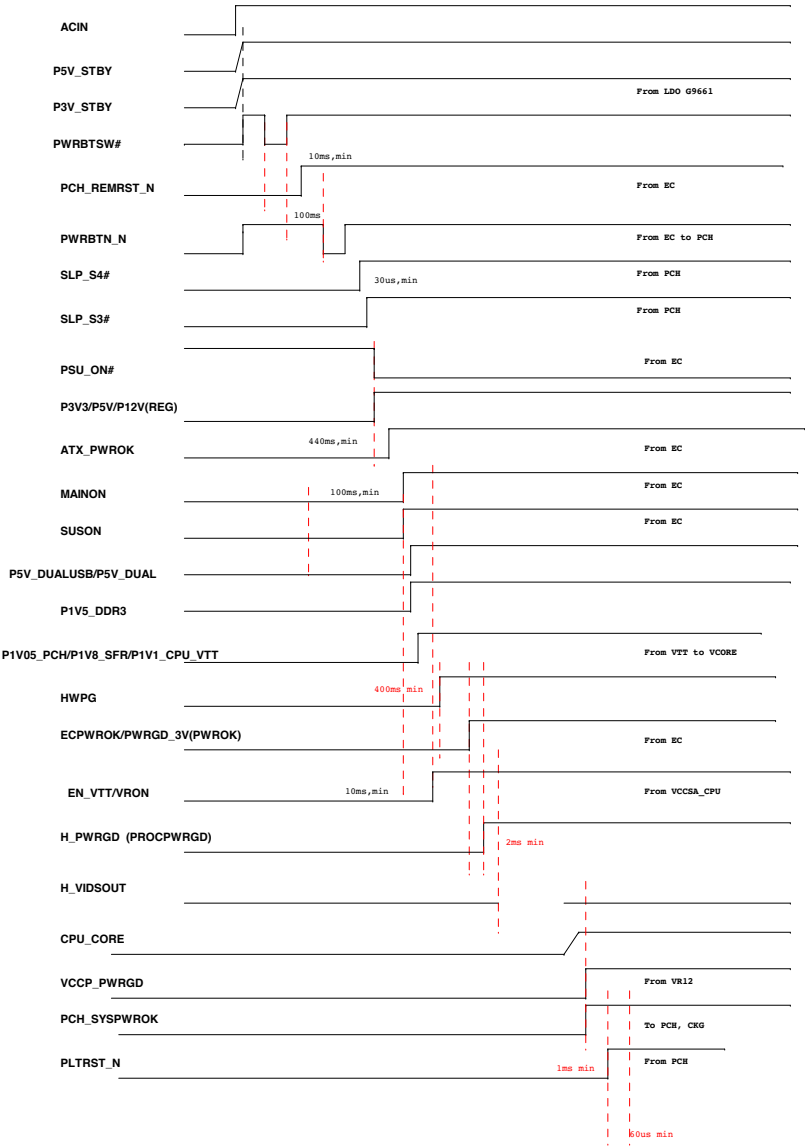
Power rail control



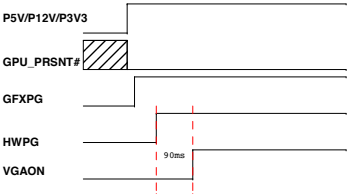
Power on Sequence



Power on Sequence :



MXM POWER ON



(10,11) M_A_DQ[63:0]

M_A_A[15:0] (10,11)

(10,11) M_A_DQS0
(10,11) M_A_DQS1
(10,11) M_A_DQS2
(10,11) M_A_DQS3
(10,11) M_A_DQS4
(10,11) M_A_DQS5
(10,11) M_A_DQS6
(10,11) M_A_DQS7

(10,11) M_A_DQS#0
(10,11) M_A_DQS#1
(10,11) M_A_DQS#2
(10,11) M_A_DQS#3
(10,11) M_A_DQS#4
(10,11) M_A_DQS#5
(10,11) M_A_DQS#6
(10,11) M_A_DQS#7

M_A_DQ0 AJ3 SA_DQ0
M_A_DQ1 AJ4 SA_DQ1
M_A_DQ2 AL3 SA_DQ2
M_A_DQ3 AL4 SA_DQ3
M_A_DQ4 AJ2 SA_DQ4
M_A_DQ5 AJ1 SA_DQ5
M_A_DQ6 AL2 SA_DQ6
M_A_DQ7 AL1 SA_DQ7
M_A_DQ8 AN1 SA_DQ8
M_A_DQ9 AN4 SA_DQ9
M_A_DQ10 AB3 SA_DQ10
M_A_DQ11 AB4 SA_DQ11
M_A_DQ12 AN2 SA_DQ12
M_A_DQ13 AN3 SA_DQ13
M_A_DQ14 AR2 SA_DQ14
M_A_DQ15 AR1 SA_DQ15
M_A_DQ16 AV2 SA_DQ16
M_A_DQ17 AW3 SA_DQ17
M_A_DQ18 AV5 SA_DQ18
M_A_DQ19 AW5 SA_DQ19
M_A_DQ20 AU2 SA_DQ20
M_A_DQ21 AU3 SA_DQ21
M_A_DQ22 AU5 SA_DQ22
M_A_DQ23 AV5 SA_DQ23
M_A_DQ24 AY7 SA_DQ24
M_A_DQ25 AU7 SA_DQ25
M_A_DQ26 AV9 SA_DQ26
M_A_DQ27 AU9 SA_DQ27
M_A_DQ28 AV7 SA_DQ28
M_A_DQ29 AW7 SA_DQ29
M_A_DQ30 AW9 SA_DQ30
M_A_DQ31 AY9 SA_DQ31
M_A_DQ32 AU35 SA_DQ32
M_A_DQ33 AW37 SA_DQ33
M_A_DQ34 AU38 SA_DQ34
M_A_DQ35 AU38 SA_DQ35
M_A_DQ36 AW35 SA_DQ36
M_A_DQ37 AY36 SA_DQ37
M_A_DQ38 AU38 SA_DQ38
M_A_DQ39 AU37 SA_DQ39
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M_A_DQ56 AG40 SA_DQ56
M_A_DQ57 AG37 SA_DQ57
M_A_DQ58 AE38 SA_DQ58
M_A_DQ59 AE37 SA_DQ59
M_A_DQ60 AG39 SA_DQ60
M_A_DQ61 AG38 SA_DQ61
M_A_DQ62 AE39 SA_DQ62
M_A_DQ63 AE40 SA_DQ63

CN7A

SA_MA_0
SA_MA_1
SA_MA_2
SA_MA_3
SA_MA_4
SA_MA_5
SA_MA_6
SA_MA_7
SA_MA_8
SA_MA_9
SA_MA_10
SA_MA_11
SA_MA_12
SA_MA_13
SA_MA_14
SA_MA_15

SA_WE_N
SA_CAS_N
SA_RAS_N

SA_BS0
SA_BS1
SA_BS2

SA_CS_N0
SA_CS_N1
SA_CS_N2
SA_CS_N3

SA_CKE0
SA_CKE1
SA_CKE2
SA_CKE3

SA_ODT0
SA_ODT1
SA_ODT2
SA_ODT3

SA_CK0
SA_CK_N0
SA_CK_N1
SA_CK_N2
SA_CK_N3

SM_DRAMRST_N

SA_DQS_8
SA_DQS_N_8

SA_ECC_CB0
SA_ECC_CB1
SA_ECC_CB2
SA_ECC_CB3
SA_ECC_CB4
SA_ECC_CB5
SA_ECC_CB6
SA_ECC_CB7

SA_DQS_N_0
SA_DQS_N_1
SA_DQS_N_2
SA_DQS_N_3
SA_DQS_N_4
SA_DQS_N_5
SA_DQS_N_6
SA_DQS_N_7

DDR_0

LGA1155

AV27 M_A_A0
AY24 M_A_A1
AW24 M_A_A2
AV23 M_A_A3
AT24 M_A_A4
AT23 M_A_A5
AU22 M_A_A6
AV22 M_A_A7
AT22 M_A_A8
AV28 M_A_A9
AU21 M_A_A10
AT21 M_A_A11
AW32 M_A_A12
AU20 M_A_A13
AT20 M_A_A14
AT20 M_A_A15

AW29 M_A_WE#
AV30 M_A_CAS#
AU28 M_A_RAS#

AY29 M_BA_A0
AW28 M_BA_A1
AV20 M_BA_A2

AU29 M_CS#_A0
AV32 M_CS#_A1
AW30 M_CS#_A2
AU33 M_CS#_A3

AV19 M_CKE_A0
AT19 M_CKE_A1
AU18 M_CKE_A2
AV18 M_CKE_A3

AV31 M_ODT_A0
AU32 M_ODT_A1
AU30 M_ODT_A2
AW33 M_ODT_A3

AY25 M_CLK_DDR_A0
AW25 M_CLK_DDR#_A0
AU24 M_CLK_DDR_A1
AU25 M_CLK_DDR#_A1
AY27 M_CLK_DDR#_A2
AV26 M_CLK_DDR_A3
AW26 M_CLK_DDR#_A3

AW18 DDR3_DRAMRST_N

AV13 M_A_DQS8
AV12 M_A_DQS#8

AU12
AU14
AW13
AY13
AU13
AU11
AY12
AW12

R58

5%

OR 4

RC0402

C94

*1U6.3V_4

DDR3_DRAMRST# (10,11,12,13)

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PROJECT: QK1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SOCKET H2 DDR3 CHANNEL A	A
Date:	Friday, April 15, 2011	Sheet 4 of 44

(12,13) M_B_DQ[63:0]

M_B_A[15:0] (12,13)

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(12,13) M_B_DQS1
(12,13) M_B_DQS2
(12,13) M_B_DQS3
(12,13) M_B_DQS4
(12,13) M_B_DQS5
(12,13) M_B_DQS6
(12,13) M_B_DQS7

(12,13) M_B_DQS#0
(12,13) M_B_DQS#1
(12,13) M_B_DQS#2
(12,13) M_B_DQS#3
(12,13) M_B_DQS#4
(12,13) M_B_DQS#5
(12,13) M_B_DQS#6
(12,13) M_B_DQS#7

M_B_DQ0 AG7
M_B_DQ1 AG8
M_B_DQ2 AJ9
M_B_DQ3 AJ8
M_B_DQ4 AG5
M_B_DQ5 AG8
M_B_DQ6 AJ6
M_B_DQ7 AJ7
M_B_DQ8 AL7
M_B_DQ9 AM7
M_B_DQ10 AM10
M_B_DQ11 AL10
M_B_DQ12 AL6
M_B_DQ13 AM6
M_B_DQ14 AL9
M_B_DQ15 AM9
M_B_DQ16 AP7
M_B_DQ17 AR7
M_B_DQ18 AP10
M_B_DQ19 AP10
M_B_DQ20 AP6
M_B_DQ21 AR6
M_B_DQ22 AP9
M_B_DQ23 AR9
M_B_DQ24 AM12
M_B_DQ25 AM13
M_B_DQ26 AR13
M_B_DQ27 AP13
M_B_DQ28 AL12
M_B_DQ29 AL13
M_B_DQ30 AP12
M_B_DQ31 AP12
M_B_DQ32 AR28
M_B_DQ33 AR29
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M_B_DQ35 AL29
M_B_DQ36 AP28
M_B_DQ37 AP29
M_B_DQ38 AM28
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M_B_DQ59 AE35
M_B_DQ60 AJ35
M_B_DQ61 AJ34
M_B_DQ62 AE33
M_B_DQ63 AE35

CN7B
SB_DQ0
SB_DQ1
SB_DQ2
SB_DQ3
SB_DQ4
SB_DQ5
SB_DQ6
SB_DQ7
SB_DQ8
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SB_DQ10
SB_DQ11
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SB_DQ63

DDR_1

LGA1155

SB_MA_0
SB_MA_1
SB_MA_2
SB_MA_3
SB_MA_4
SB_MA_5
SB_MA_6
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SB_WE_N
SB_CAS_N
SB_RAS_N
SB_CS_N0
SB_CS_N1
SB_CS_N2
SB_CS_N3
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SB_CKE1
SB_CKE2
SB_CKE3
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SB_ODT1
SB_ODT2
SB_ODT3
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SB_CLK_N0
SB_CLK1
SB_CLK_N1
SB_CLK2
SB_CLK_N2
SB_CLK3
SB_CLK_N3
SB_DQS_8
SB_DQS_N_8
SB_ECC_CB0
SB_ECC_CB1
SB_ECC_CB2
SB_ECC_CB3
SB_ECC_CB4
SB_ECC_CB5
SB_ECC_CB6
SB_ECC_CB7

AK24 M_B_A0
AM20 M_B_A1
AM19 M_B_A2
AK18 M_B_A3
AP19 M_B_A4
AP18 M_B_A5
AM18 M_B_A6
AL18 M_B_A7
AN18 M_B_A8
AY17 M_B_A9
AN23 M_B_A10
AU17 M_B_A11
AT18 M_B_A12
AR26 M_B_A13
AY16 M_B_A14
AV16 M_B_A15

AR25 M_B_WE#
AK25 M_B_CAS#
AP24 M_B_RAS#

AP23 M_BA_B0
AM24 M_BA_B1
AW17 M_BA_B2

AN25 M_CS#_B0
AN26 M_CS#_B1
AL25 M_CS#_B2
AT26 M_CS#_B3

AU16 M_CKE_B0
AY15 M_CKE_B1
AW15 M_CKE_B2
AV15 M_CKE_B3

AL26 M_ODT_B0
AP26 M_ODT_B1
AM26 M_ODT_B2
AK26 M_ODT_B3

AL21 M_CLK_DDR_B0
AL22 M_CLK_DDR#_B0
AL20 M_CLK_DDR#_B1
AL23 M_CLK_DDR_B2
AM22 M_CLK_DDR#_B2
AP21 M_CLK_DDR_B3
AN21 M_CLK_DDR#_B3

AN16 M_B_DQS8
AN15 M_B_DQS#8

AL16
AM16
AP16
AR16
AL15
AM15
AR15
AP15

M_B_WE# (12,13)
M_B_CAS# (12,13)
M_B_RAS# (12,13)

M_BA_B0 (12,13)
M_BA_B1 (12,13)
M_BA_B2 (12,13)

M_CS#_B0 (12)
M_CS#_B1 (12)
M_CS#_B2 (13)
M_CS#_B3 (13)

M_CKE_B0 (12)
M_CKE_B1 (12)
M_CKE_B2 (13)
M_CKE_B3 (13)

M_ODT_B0 (12)
M_ODT_B1 (12)
M_ODT_B2 (13)
M_ODT_B3 (13)

M_CLK_DDR_B0 (12)
M_CLK_DDR#_B0 (12)
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TP107
TP106

PROPRIETARY NOTE

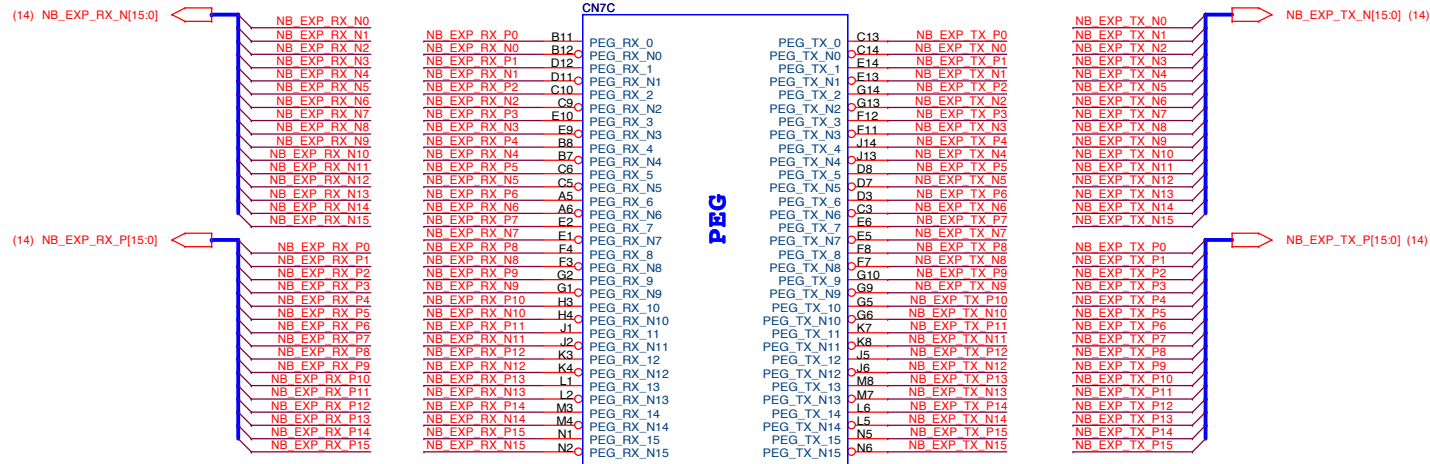
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PROJECT: QK1

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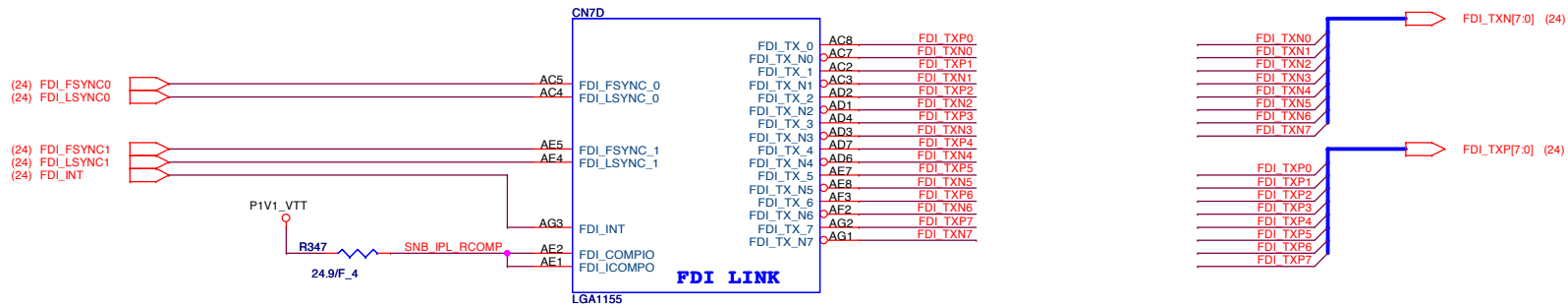
Size	Document Number	Rev
Custom	SOCKET H2 DDR3 CHANNEL B	A
Date:	Friday, April 15, 2011	Sheet 5 of 44



FDI DISABLE GUIDELINES (FROM PDG)

FDI SIGNAL	RECOMMENDATION
FDI_TX[7:0]	FLOAT
FDI_TX_N[7:0]	FLOAT
FDI_FSYNC	1K RESISTOR TO VCC_FDI OR VSS
FDI_LSYNC	1K RESISTOR TO VCC_FDI OR VSS
FDI_INT	1K RESISTOR TO VCC_FDI OR VSS

CAD NOTE:
 PIN B5 ROUTING TO RESISTOR NEED TO BE 5 MILS
 PIN C4 AND B4 ROUTING TO RESISTOR NEED TO BE 4 MILS
 THERE ARE SPACING RULES ALSO - CHECK RULES DOCUMENT

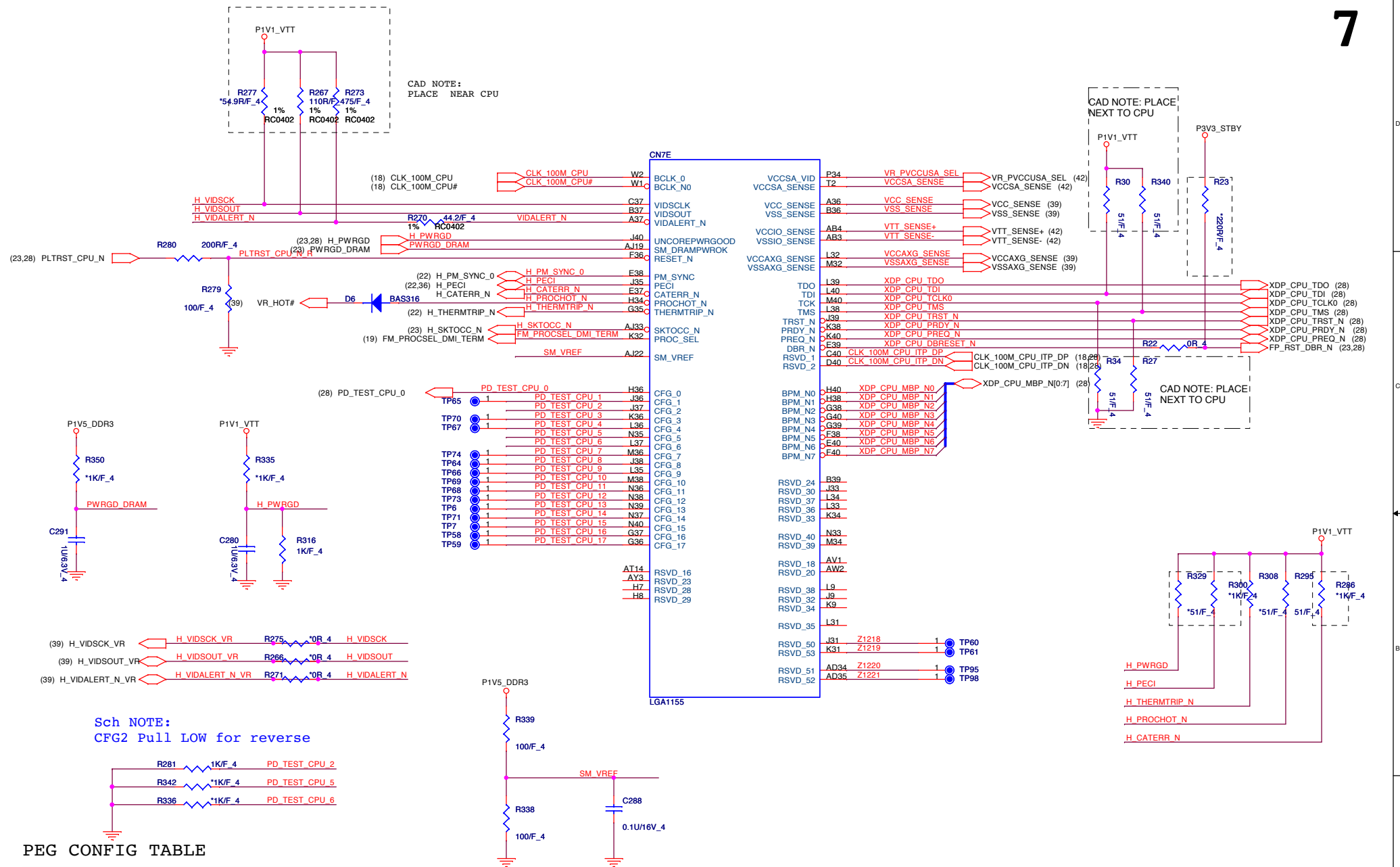


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PROJECT: QK1
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Size	Document Number	Rev
Custom	SOCKET H2 PCIE, DMI	A
Date:	Friday, April 15, 2011	Sheet 6 of 44

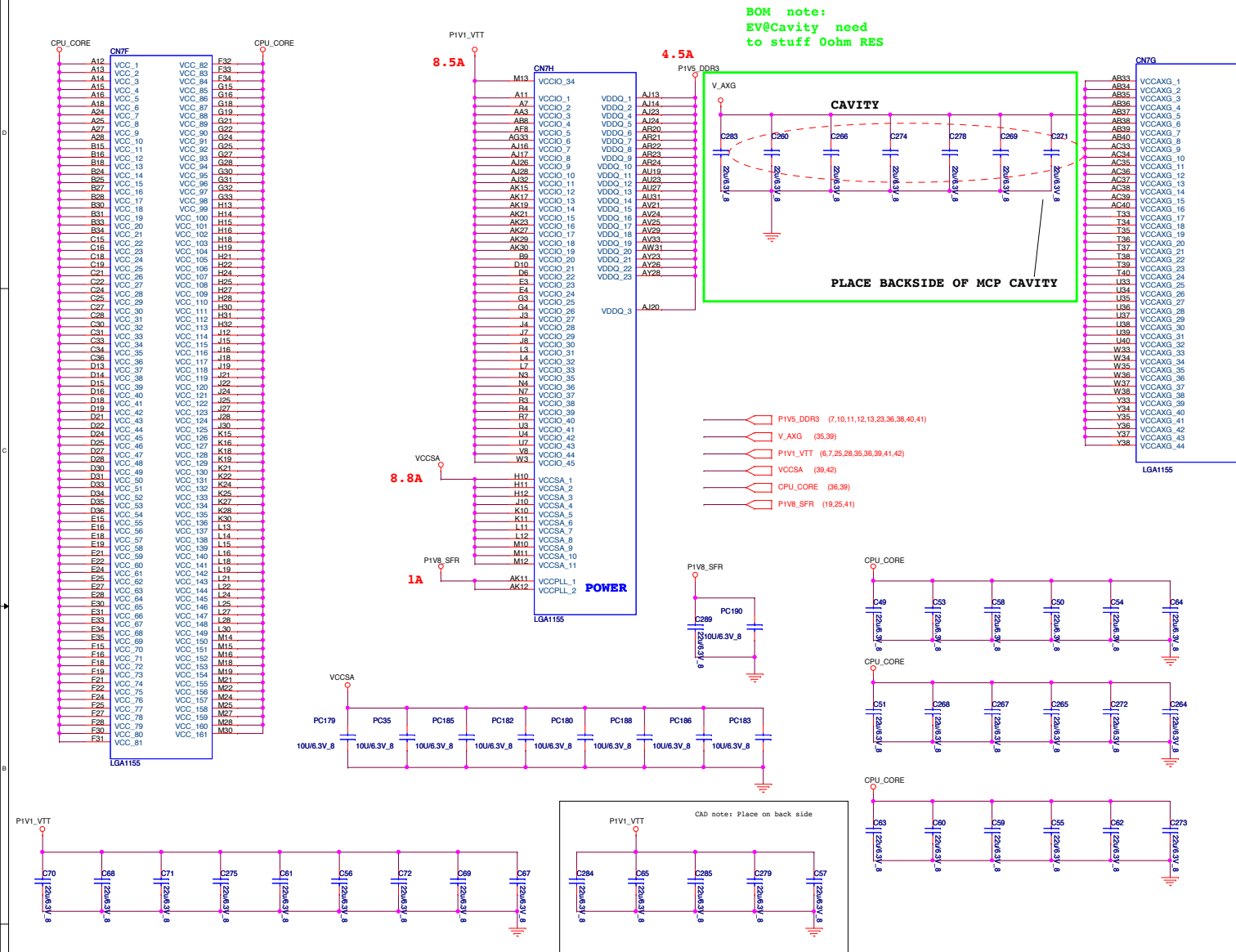


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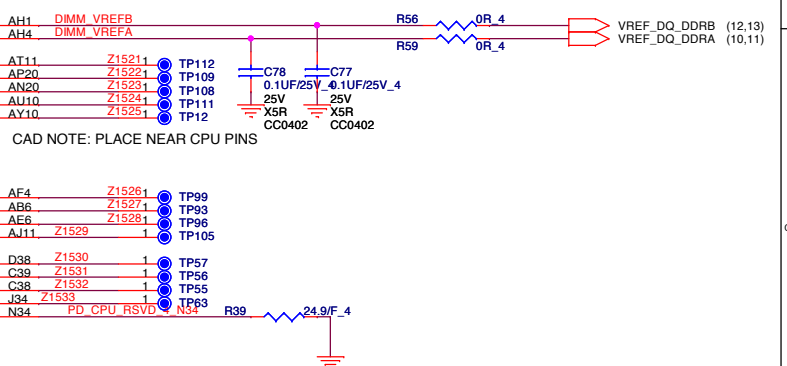
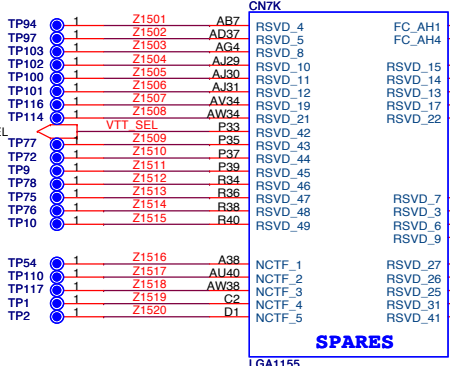


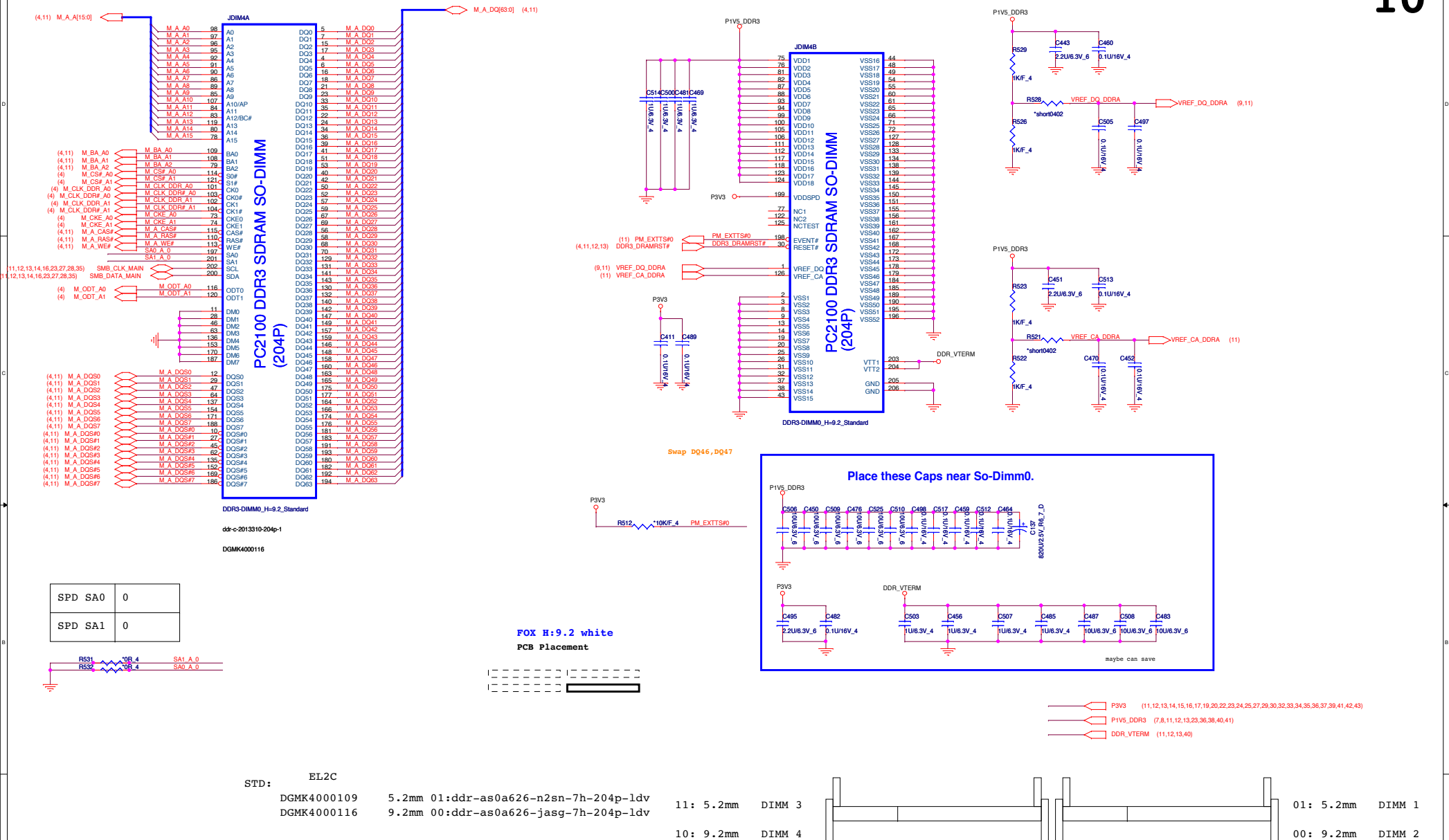
PROJECT: QK1
Quanta Computer Inc.

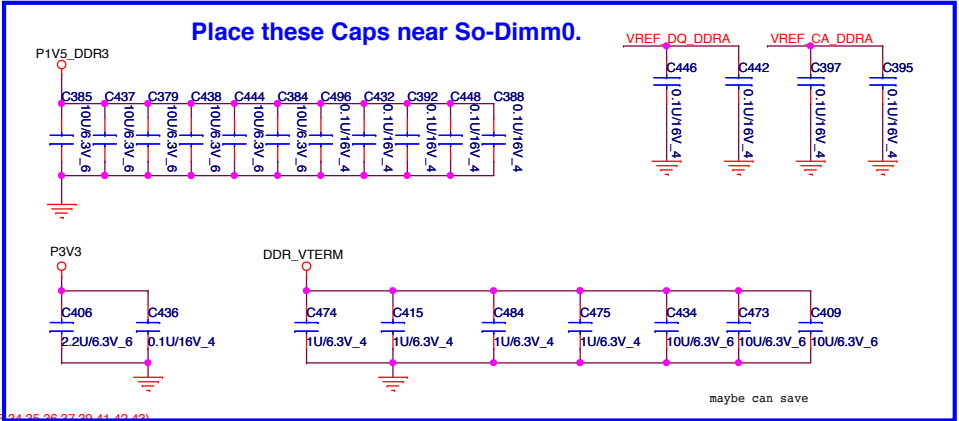
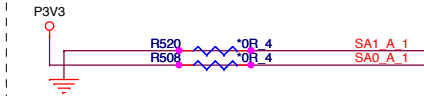
Size	Document Number	Rev
Custom	SOCKET H2 CLK, CTRL, MISC, DE	A
Date:	Friday, April 15, 2011	Sheet 7 of 44



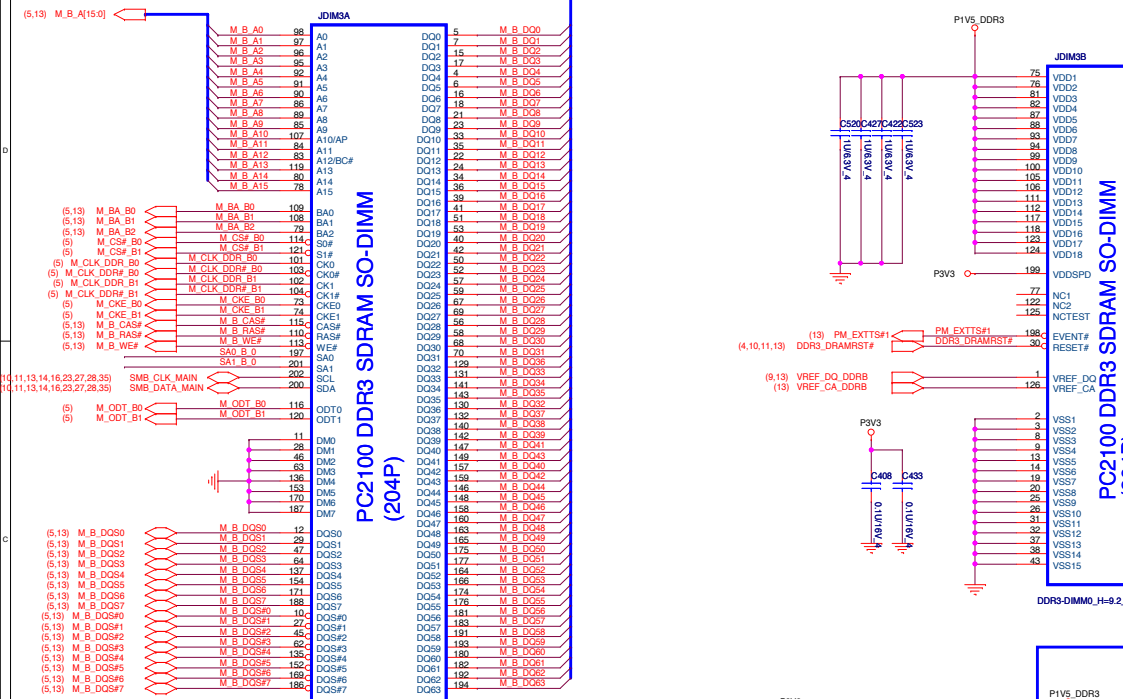
CN71			CN7J		
A17	VSS_1	AM27	AV11	VSS_181	G8
A23	VSS_2	AM3	AV14	VSS_182	H1
A26	VSS_3	AM30	AV17	VSS_183	H17
A29	VSS_4	AM36	AV3	VSS_184	H2
A35	VSS_5	AM37	AV35	VSS_185	H20
AA33	VSS_6	AM38	AV38	VSS_186	H23
AA34	VSS_7	AM39	AV6	VSS_187	H26
AA35	VSS_8	AM4	AW10	VSS_188	H29
AA36	VSS_9	AM40	AW11	VSS_189	H33
AA37	VSS_10	AM5	AW14	VSS_190	H35
AA38	VSS_11	AN10	AW16	VSS_191	H37
AA6	VSS_12	AN11	AW36	VSS_192	H39
AB5	VSS_13	AN14	AW6	VSS_193	H5
AC1	VSS_14	AN17	AY11	VSS_194	H6
AC6	VSS_15	AN19	AY14	VSS_195	H9
AD33	VSS_16	AN22	AY18	VSS_196	J11
AD36	VSS_17	AN24	AY35	VSS_197	J17
AD38	VSS_18	AN27	AY4	VSS_198	J20
AD39	VSS_19	AN30	AY6	VSS_199	J23
AD5	VSS_20	AN32	AY8	VSS_200	J26
AD8	VSS_21	AN33	B10	VSS_201	J29
AE3	VSS_22	AN34	B13	VSS_202	J32
AE33	VSS_23	AN35	B14	VSS_203	K1
AE36	VSS_24	AN36	B17	VSS_204	K12
AF1	VSS_25	AN5	B23	VSS_205	K13
AF34	VSS_26	AN6	B26	VSS_206	K14
AF36	VSS_27	AN7	B29	VSS_207	K17
AF37	VSS_28	AN8	B32	VSS_208	K2
AF40	VSS_29	AN9	B35	VSS_209	K20
AF5	VSS_30	AN9	B38	VSS_210	K23
AF6	VSS_31	AP1	B6	VSS_211	K26
AF7	VSS_32	AP11	C11	VSS_212	K29
AG36	VSS_33	AP12	C12	VSS_213	K33
AH2	VSS_34	AP14	C17	VSS_214	K35
AH3	VSS_35	AP17	C20	VSS_215	K37
AH33	VSS_36	AP22	C23	VSS_216	K39
AH36	VSS_37	AP25	C26	VSS_217	K5
AH37	VSS_38	AP27	C29	VSS_218	K6
AH38	VSS_39	AP30	C32	VSS_219	L10
AH39	VSS_40	AP36	C35	VSS_220	L17
AH40	VSS_41	AP37	C7	VSS_221	L20
AH5	VSS_42	AP40	C8	VSS_222	L23
AH8	VSS_43	AP45	D17	VSS_223	L29
AJ12	VSS_44	AR11	D2	VSS_224	L8
AJ15	VSS_45	AR14	D20	VSS_225	L1
AJ18	VSS_46	AR17	D23	VSS_226	M1
AJ21	VSS_47	AR18	D26	VSS_227	M17
AJ25	VSS_48	AR19	D29	VSS_228	M2
AJ27	VSS_49	AR27	D32	VSS_229	M20
AJ36	VSS_50	AR30	D37	VSS_230	M23
AJ5	VSS_51	AR36	D39	VSS_231	M26
AK1	VSS_52	AR5	D4	VSS_232	M29
AK10	VSS_53	AT1	D5	VSS_233	M33
AK13	VSS_54	AT10	D9	VSS_234	M35
AK14	VSS_55	AT12	E11	VSS_235	M37
AK16	VSS_56	AT13	E12	VSS_236	M39
AK22	VSS_57	AT15	E17	VSS_237	M5
AK28	VSS_58	AT16	E20	VSS_238	M6
AK31	VSS_59	AT17	E23	VSS_239	M9
AK32	VSS_60	AT2	E26	VSS_240	N8
AK33	VSS_61	AT25	E29	VSS_241	P1
AK34	VSS_62	AT27	E32	VSS_242	P2
AK35	VSS_63	AT28	E36	VSS_243	P36
AK36	VSS_64	AT29	E7	VSS_244	P38
AK37	VSS_65	AT3	E8	VSS_245	P40
AK4	VSS_66	AT30	F1	VSS_246	P5
AK40	VSS_67	AT31	F10	VSS_247	P6
AK5	VSS_68	AT32	F13	VSS_248	P33
AK6	VSS_69	AT33	F14	VSS_249	P35
AK7	VSS_70	AT34	F17	VSS_250	P37
AK8	VSS_71	AT35	F2	VSS_251	P39
AK9	VSS_72	AT36	F20	VSS_252	P8
AL11	VSS_73	AT37	F23	VSS_253	T1
AL14	VSS_74	AT38	F26	VSS_254	T5
AL17	VSS_75	AT39	F29	VSS_255	T6
AL19	VSS_76	AT4	F35	VSS_256	U8
AL24	VSS_77	AT40	F37	VSS_257	V1
AL27	VSS_78	AT5	F39	VSS_258	V2
AL30	VSS_79	AT6	F5	VSS_259	V33
AL36	VSS_80	AT9	F6	VSS_260	V34
AL5	VSS_81	AT9	F9	VSS_261	V35
AM1	VSS_82	AU1	G11	VSS_262	V36
AM11	VSS_83	AU15	G12	VSS_263	V37
AM14	VSS_84	AU26	G17	VSS_264	V38
AM17	VSS_85	AU34	G20	VSS_265	V39
AM2	VSS_86	AU4	G23	VSS_266	V40
AM21	VSS_87	AU6	G26	VSS_267	V5
AM23	VSS_88	AU8	G29	VSS_268	W6
AM25	VSS_89	AV10	G34	VSS_269	Y5
A4	VSS_90	AV39	G7	VSS_270	Y8
VSS_NCTF_1 VSS_NCTF_2			AY37	VSS_NCTF_3	B3
VSS_NCTF_4					





[illegible]

CHANNEL B DIMM 2



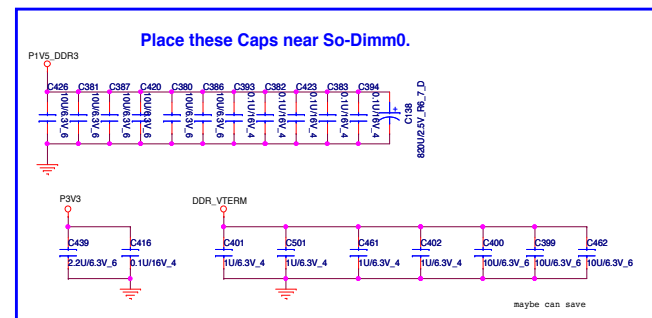
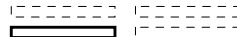
H_B_DQ32-----JDIM4.130-----JDIM3.130
H_B_DQ36-----JDIM4.129-----JDIM3.129
H_B_DQ41-----JDIM4.147-----JDIM3.147
H_B_DQ43-----JDIM4.149-----JDIM3.149
H_B_DQ42-----JDIM4.159-----JDIM3.159
H_B_DQ40-----JDIM4.157-----JDIM3.157

SPD SA0	0
SPD SA1	1

P3V3 R538 R534 OR_4 SA0_B_0
R534 OR_4 SA1_B_0

P3V3 (10,11,13,14,15,16,17,19,20,22,23,24,25,27,29,30,32,33,34,35,36,37,39,41,42,43)
P1V5_DDR3 (7,8,10,11,13,23,36,38,40,41)
DDR_VTERM (10,11,13,40)

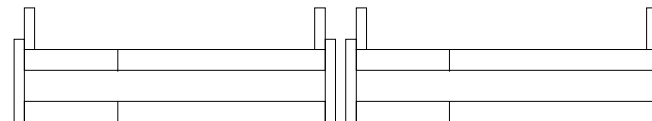
SUYIN H:9.2 Black
PCB Placement



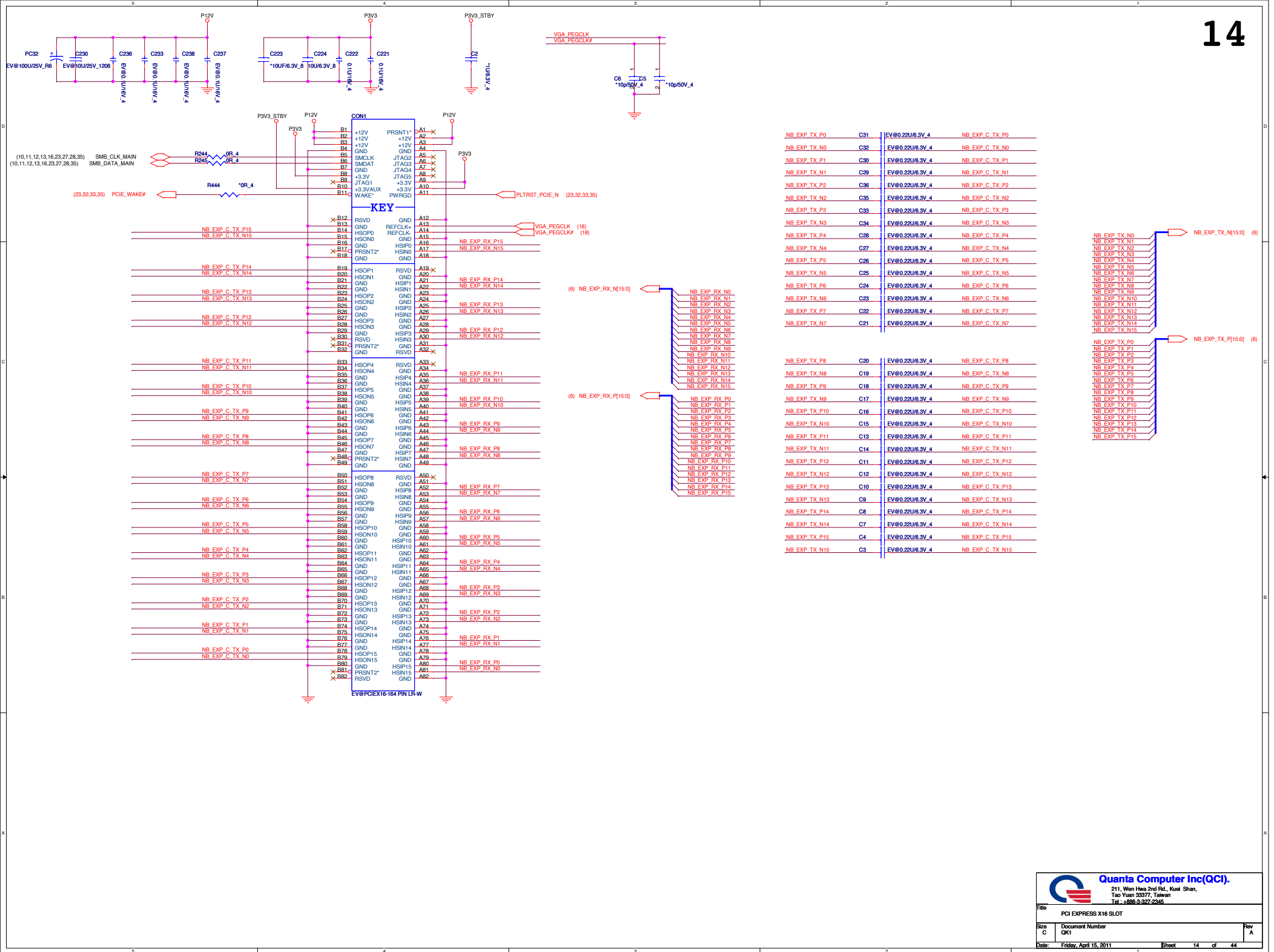
STD: EL2C

DGMK4000109 DGMK4000155 5.2mm 01:ddr-as0a626-n2sn-7h-204p-ldv
DGMK4000116 DGMK4000157 9.2mm 00:ddr-as0a626-jasg-7h-204p-ldv

11: 5.2mm DIMM 3
10: 9.2mm DIMM 4

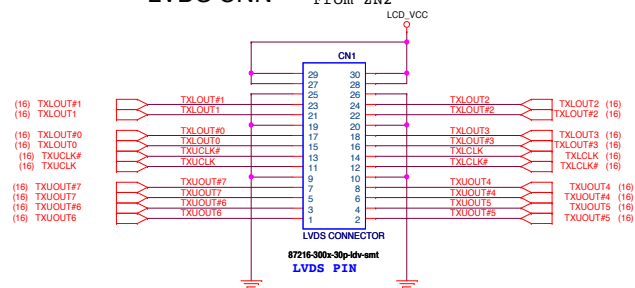


01: 5.2mm DIMM 1
00: 9.2mm DIMM 2

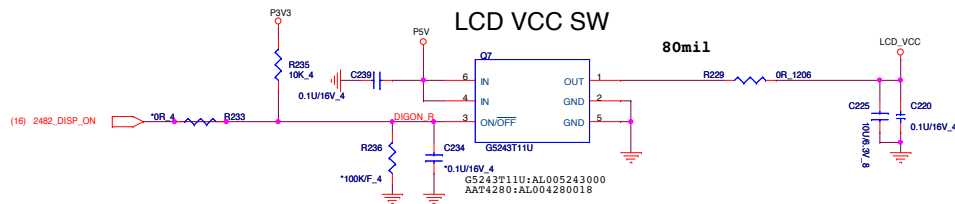


LVDS CNN

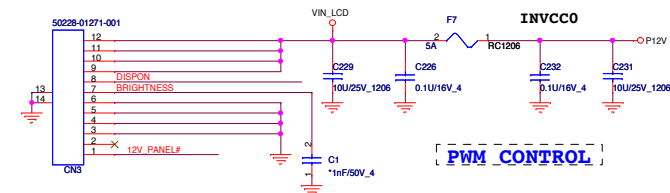
From ZN2



LCD VCC SW



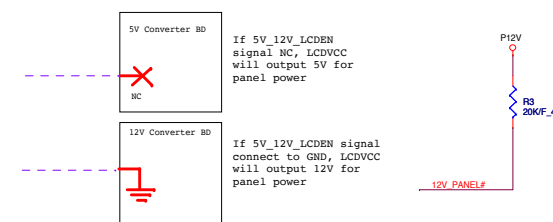
TO Converter Board



Change CN18 Footprint to 12pin for add 5V/12V Panel ID, 1/8 Max

BKLTEN Delay 2ms after ECPWROK.

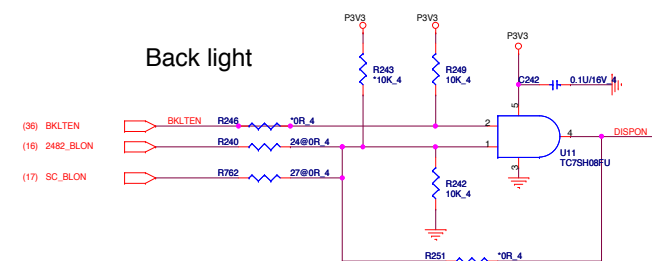
From EC Control



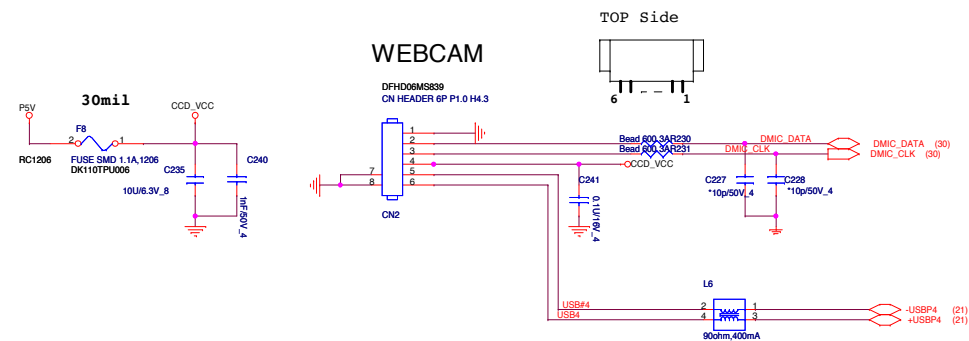
Brightnrss

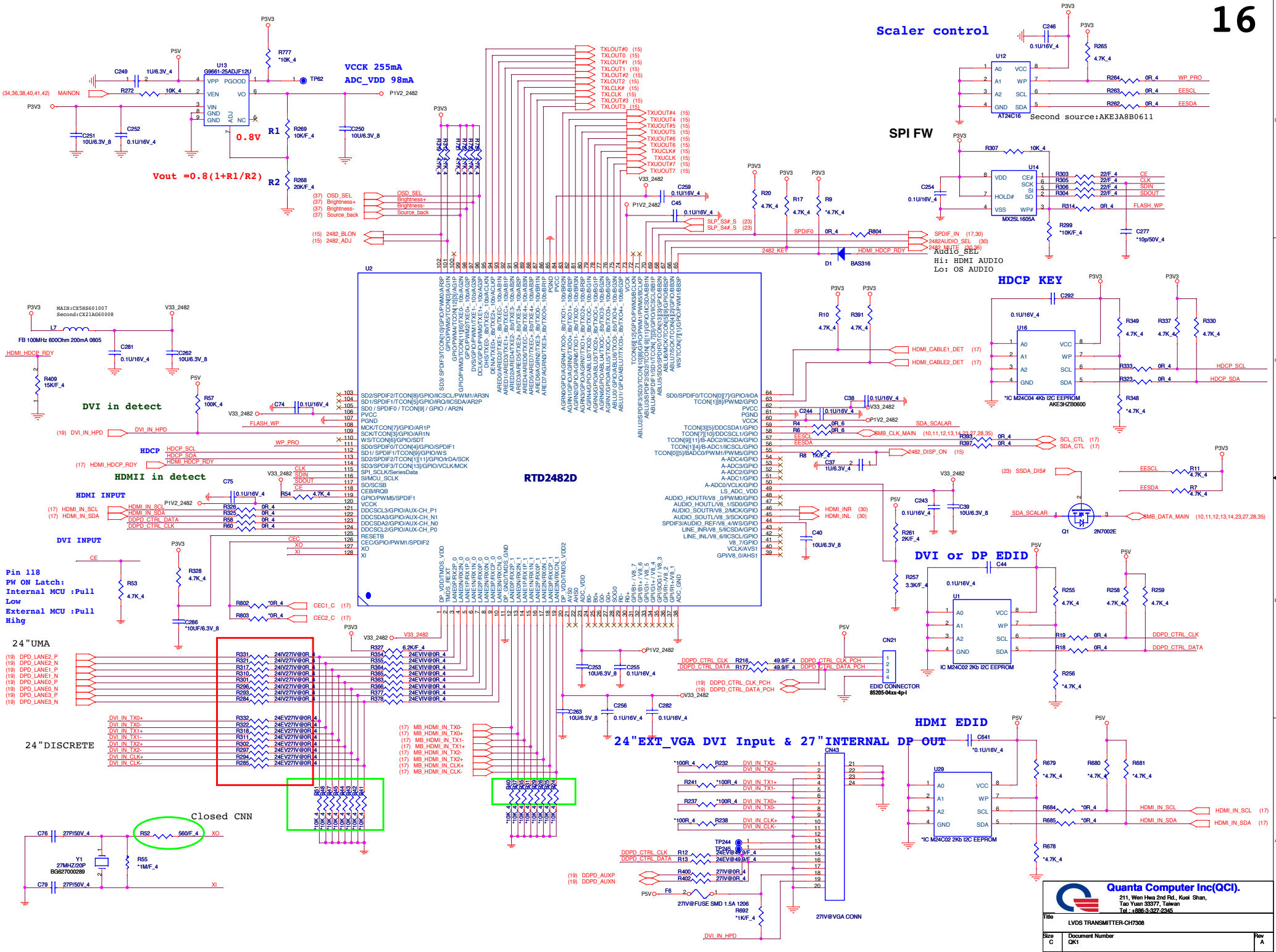


Back light

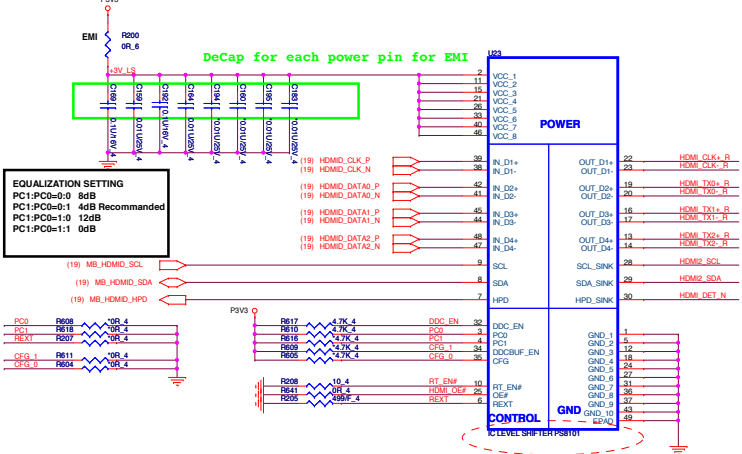


WEBCAM

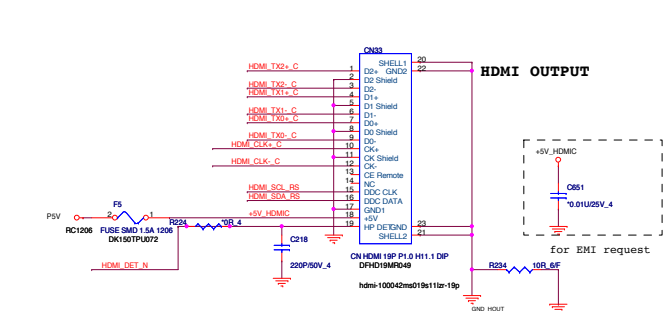
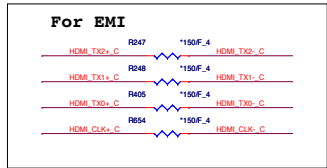




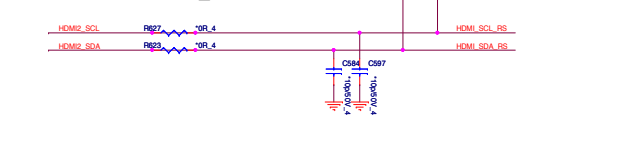
HDMI OUT



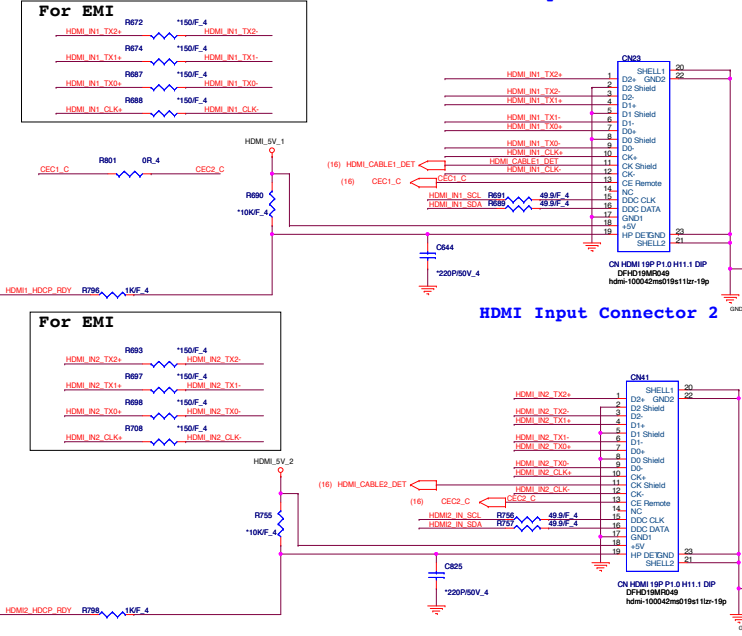
Mount for Non-EXT_VGA Option.



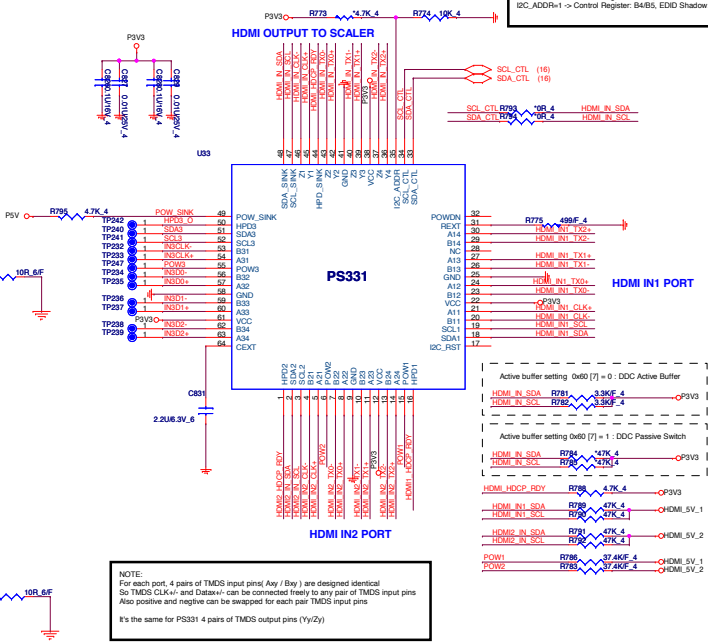
Mount for Non-EXT_VGA Option.



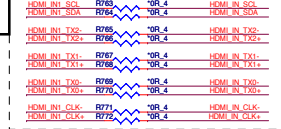
HDMI INPUT CONN



HDMI INPUT SWITCH IC

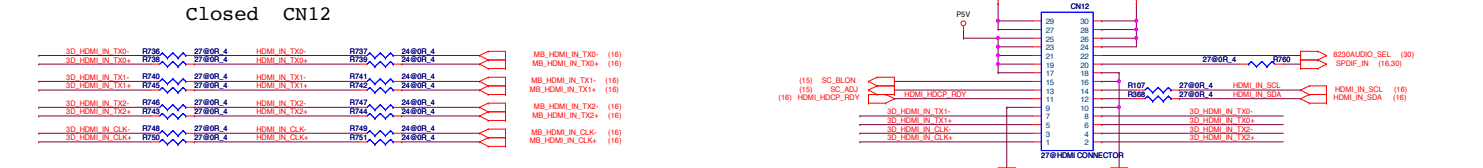


ONLY 1 PORT HDMI INPUT



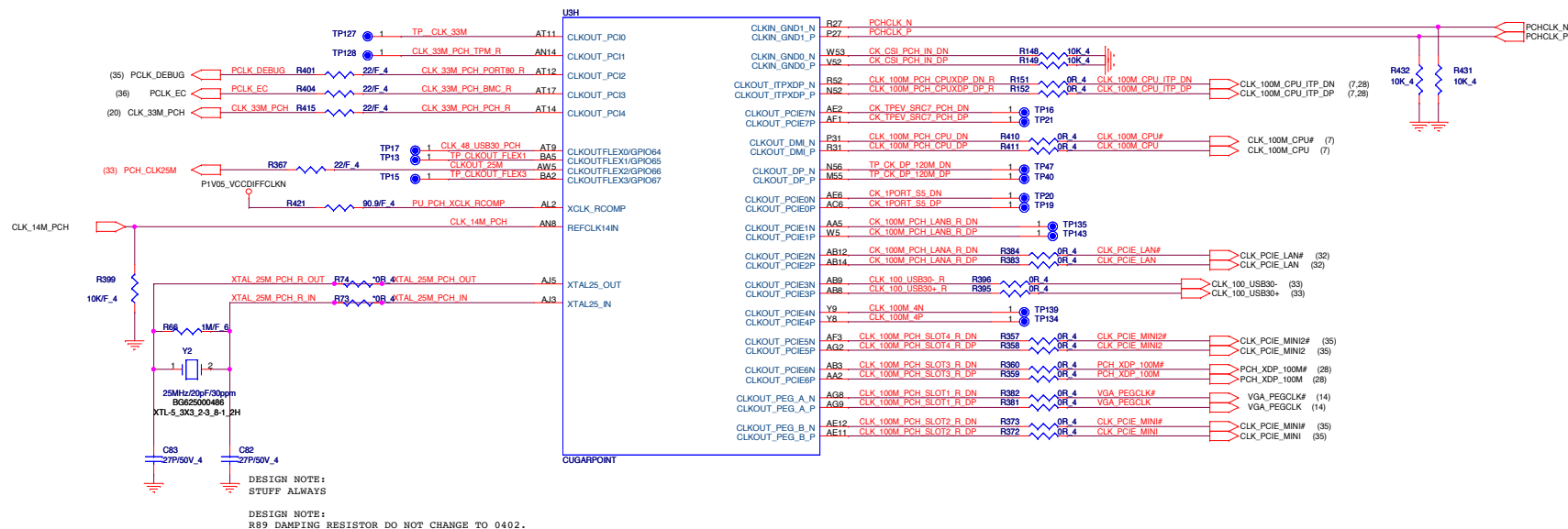
HDMI INPUT

HDMI INPUT to Scaler/B



HDMI input and Scalar/B control

COPY FROM LVDS CONN 30P



CAD NOTE:
PLACE RESISTORS NEAR CPU AND XDP HEADER AND OVERLAP COMMON PAD

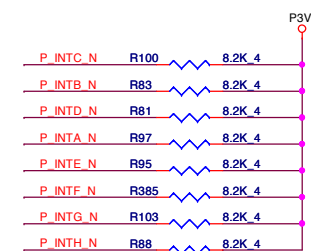
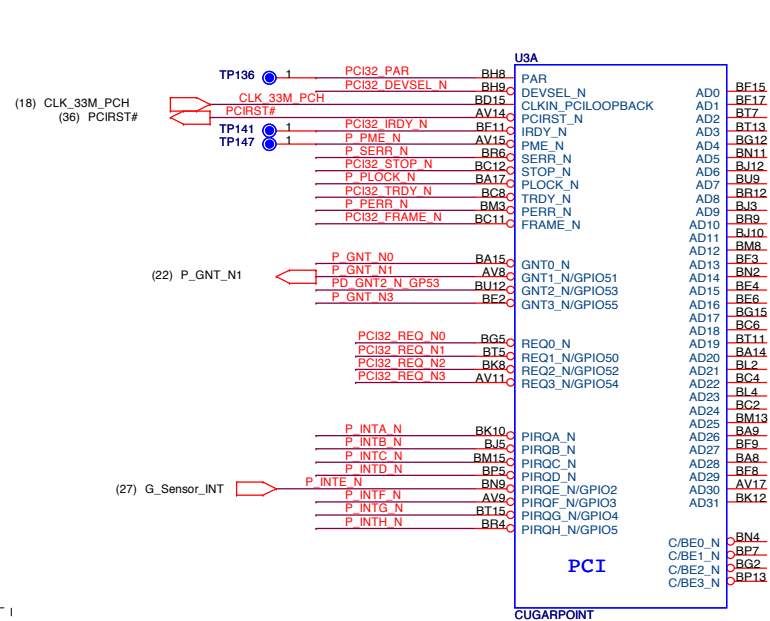
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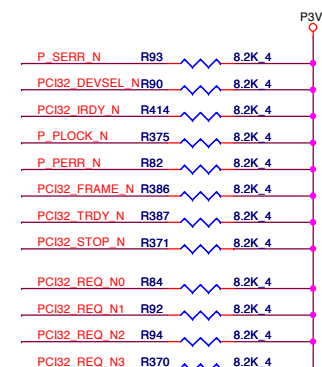


PROJECT: QK1
Quanta Computer Inc.

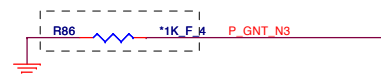
Size C	Document Number PCH-CLOCK DISTRIBUTION	Rev A
Date: Friday, April 15, 2011	Sheet 18 of 44	



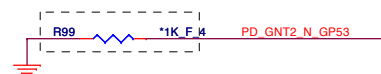
PCI PULL-UPS



DESIGN NOTE:
STRAPPING OPTION PIN DIFFERENCE
FOR BIOS BOOT DEVICE SELECTION
WHEN USING ZIGZAG
PCH(1B) PROVIDES INTERNAL P/U (DEFAULT) CHOSEN



DESIGN NOTE:
A16 SWAP OVERRIDE OVERRIDE IF SAMPLED LOW



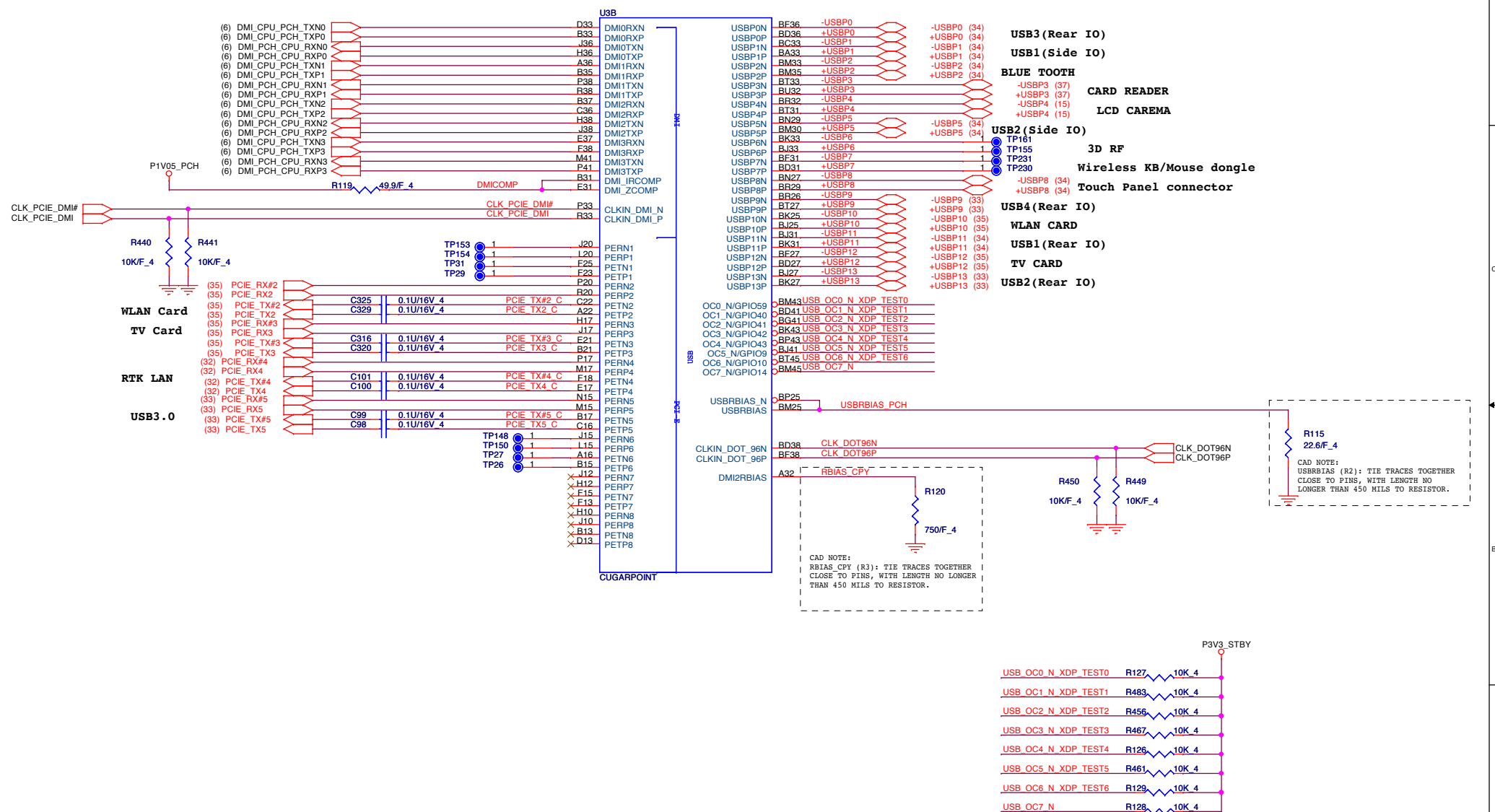
DESIGN NOTE:
DMI AC (FULL SWING) OR DC (HALF SWING) COUPLING MODE
P/U: DMI DC COUPLING MODE ENABLED (DEFAULT)
P/D: DMI AC COUPLING MODE ENABLED
PCH PROVIDES WEAK INTERNAL P/U

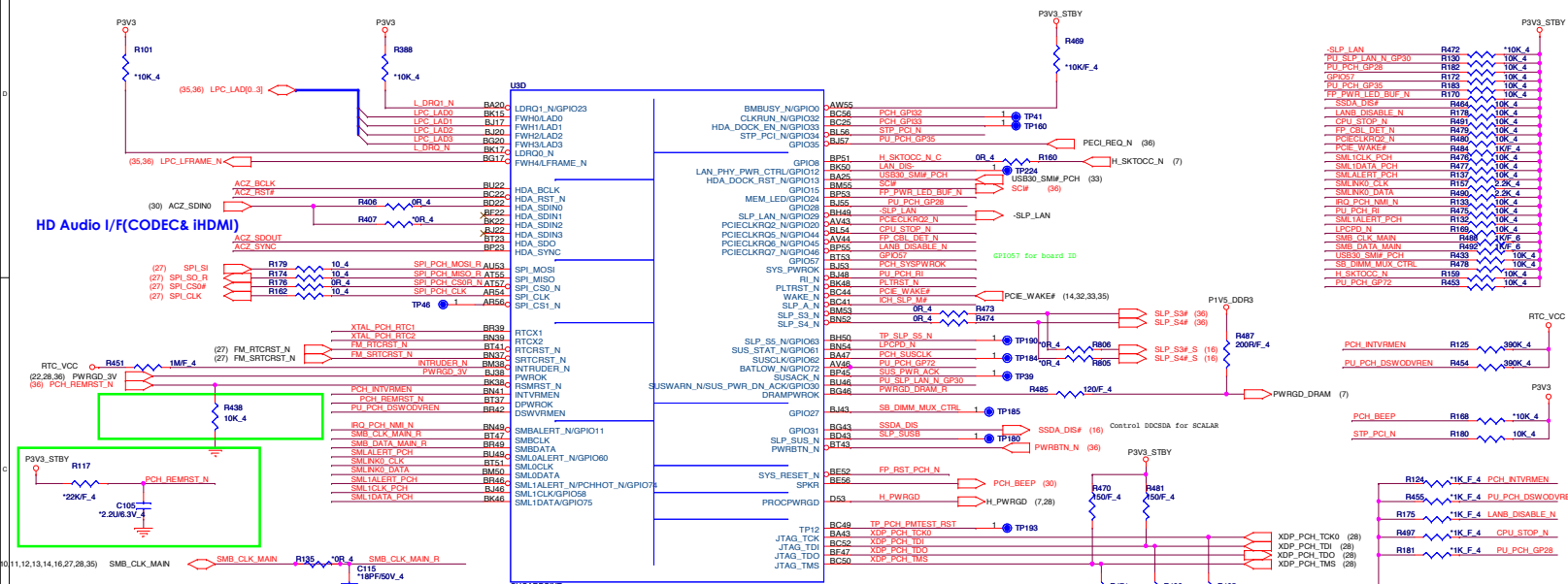
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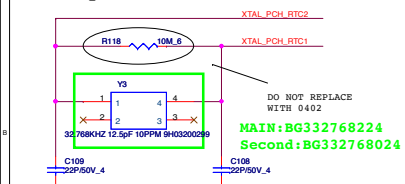
PROJECT: QK1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH-PCI	A
Date:	Friday, April 15, 2011	Sheet 20 of 44

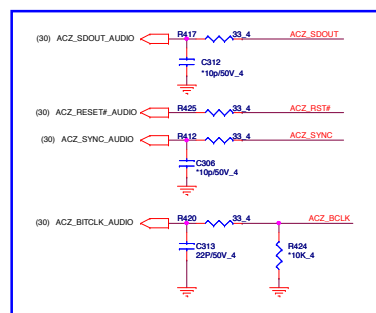




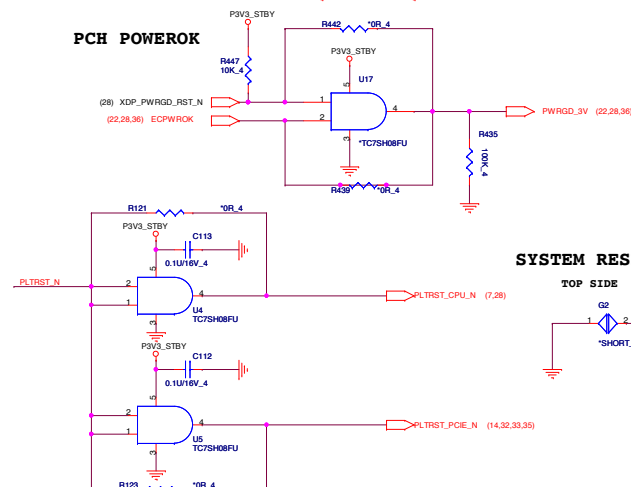
Crystal 32.768KHz



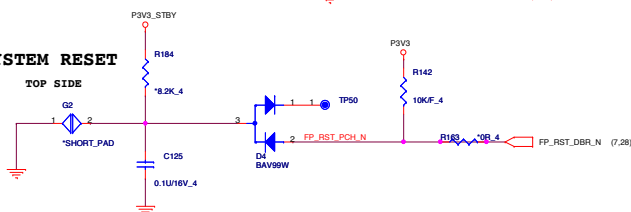
To Azalia



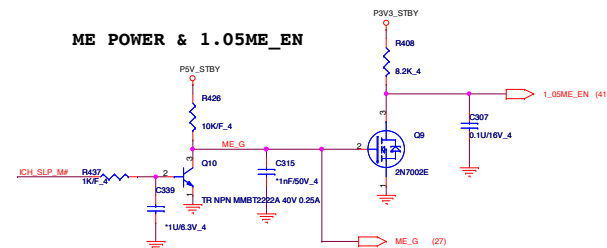
PCH POWEROK



SYSTEM RESET



ME POWER & 1.05ME EN



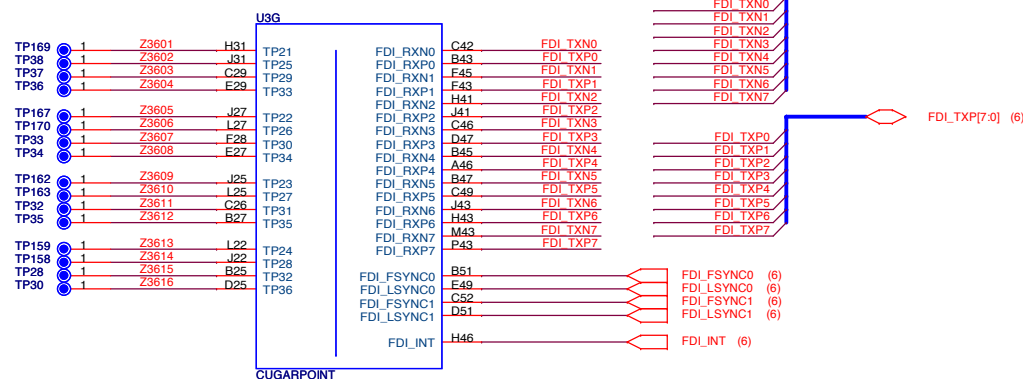
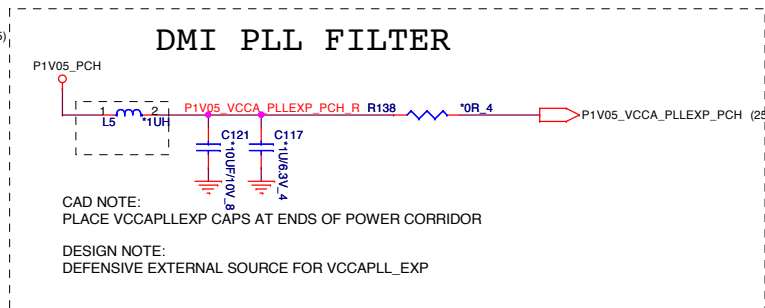
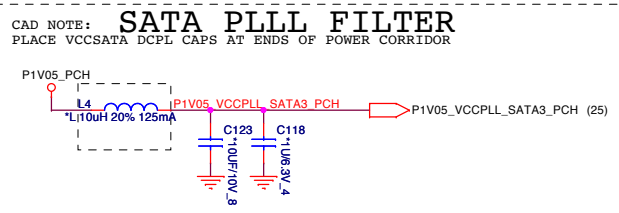
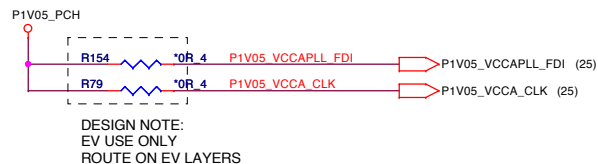
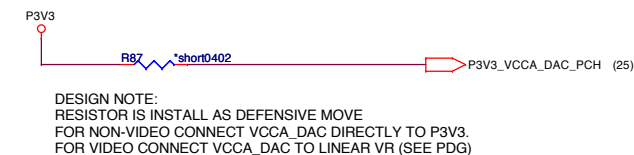
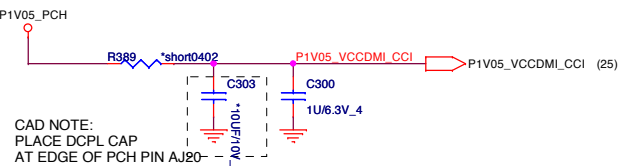
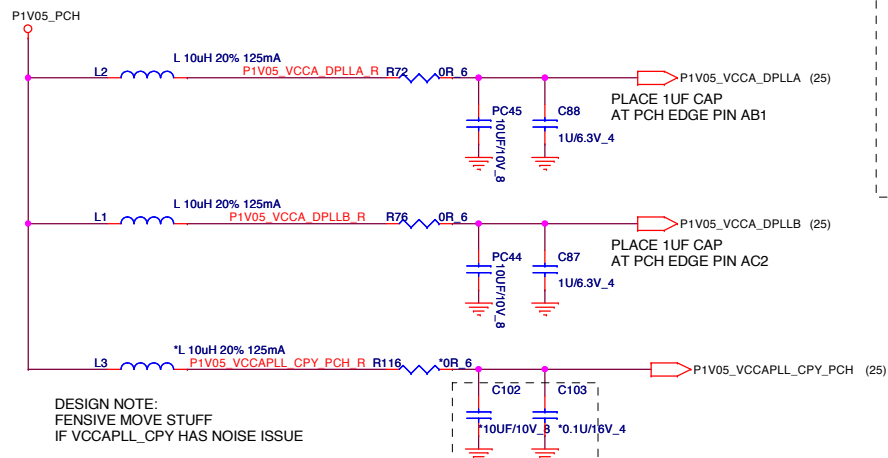
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PROJECT: QK1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH-MISC, GPIO, SMBUS, LPC	A
Date:	Friday, April 15, 2011	Sheet 23 of 44

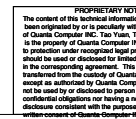


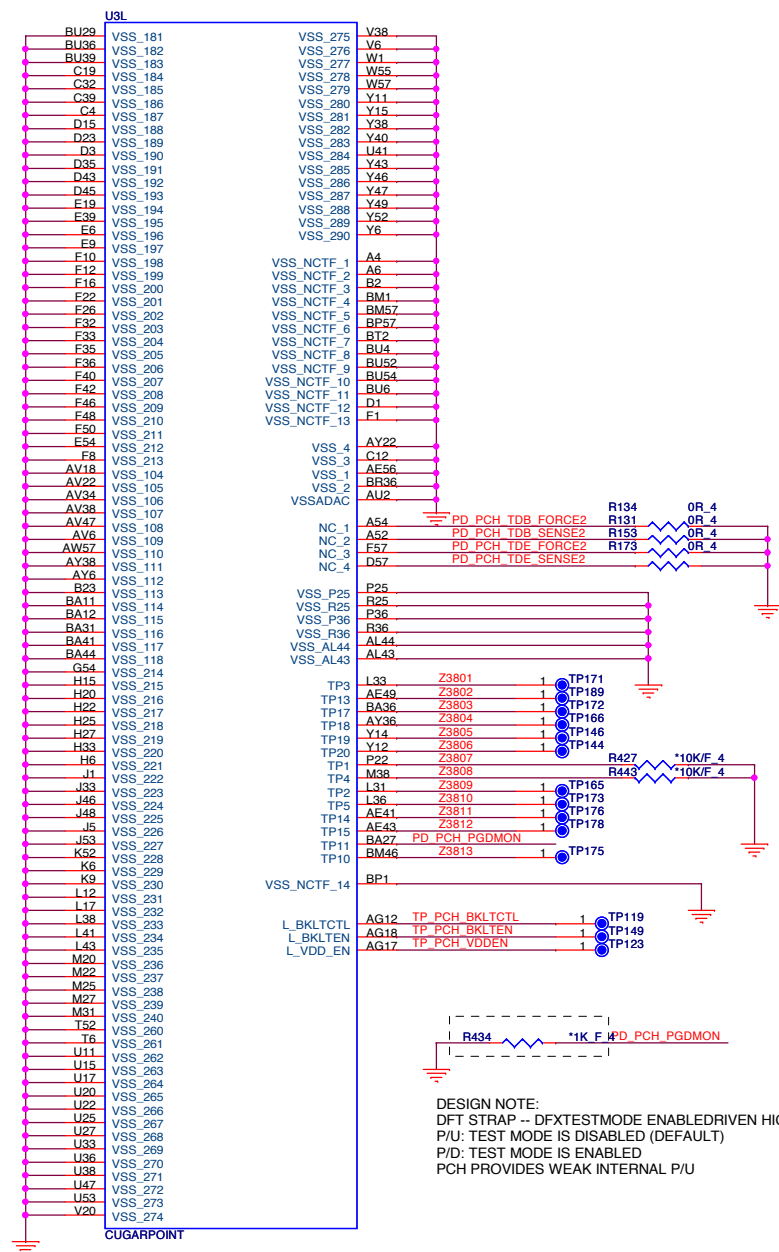
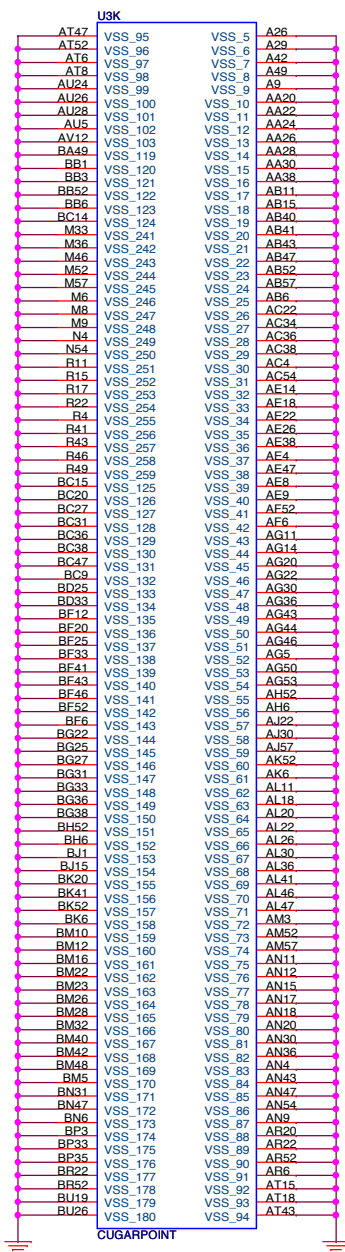
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PROJECT: QK1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH-PLL FILTERS	A
Date:	Friday, April 15, 2011	Sheet 24 of 44





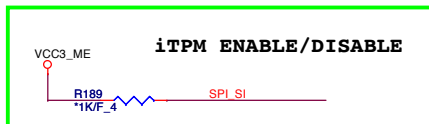
DESIGN NOTE:
DFT STRAP -- DFTTESTMODE ENABLEDRIVEN HIGH OR LOW
P/U: TEST MODE IS DISABLED (DEFAULT)
P/D: TEST MODE IS ENABLED
PCH PROVIDES WEAK INTERNAL P/U

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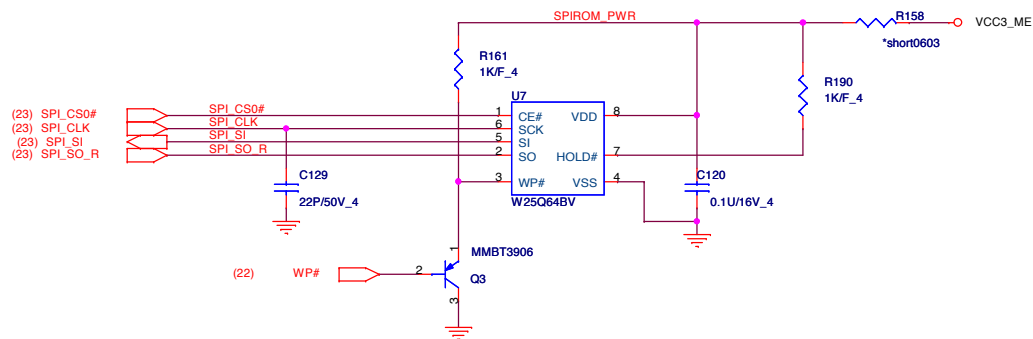


PROJECT: QK1
Quanta Computer Inc.

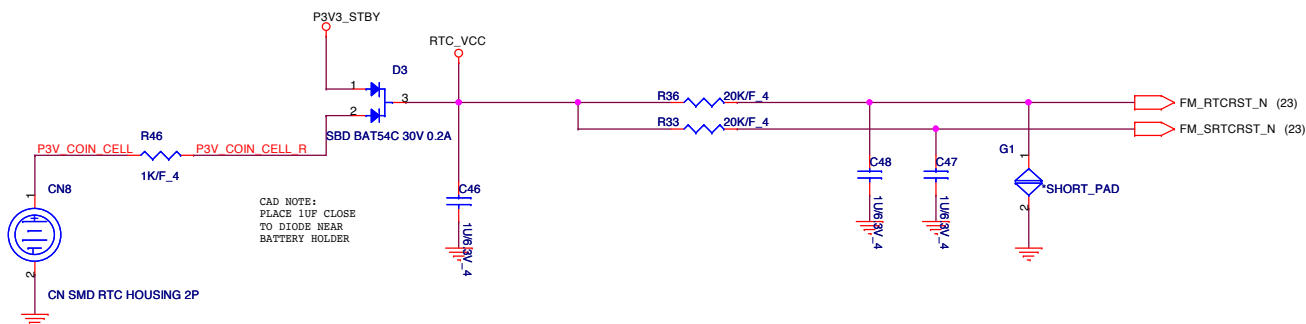
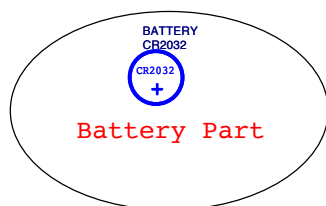
Size	Document Number	Rev
Custom	PCH-GND	A
Date:	Thursday, April 07, 2011	Sheet 26 of 44



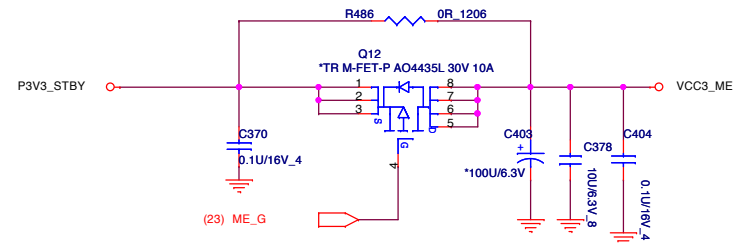
PCH SPI ROM(8MB)



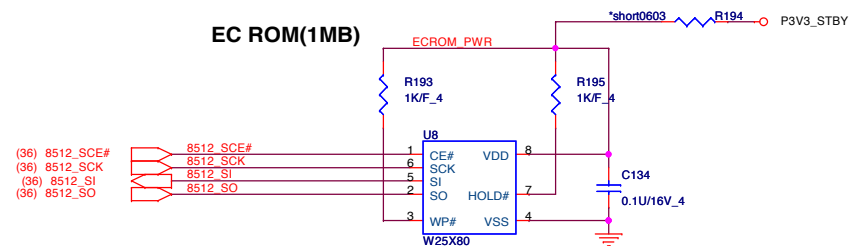
COIN CELL BATTERY



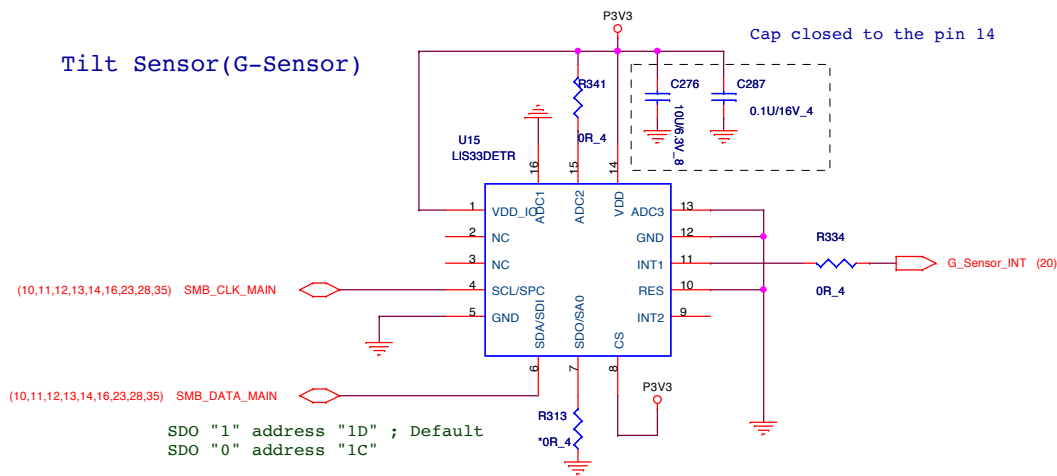
Mount R486 for Non-M3 support



EC ROM(1MB)



Tilt Sensor(G-Sensor)



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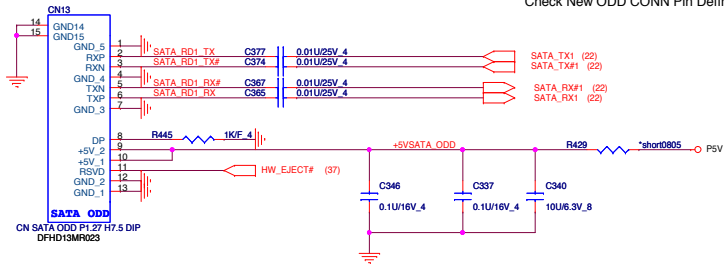
PROJECT: QK1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RSM_RST AND BATTERY	A
Date:	Friday, April 15, 2011	Sheet 27 of 44

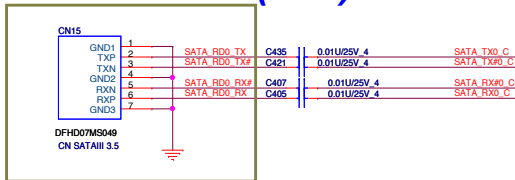
SATA ODD

Copy from EL5

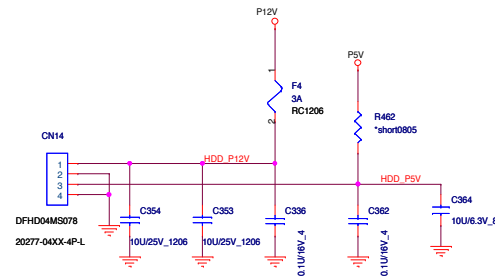
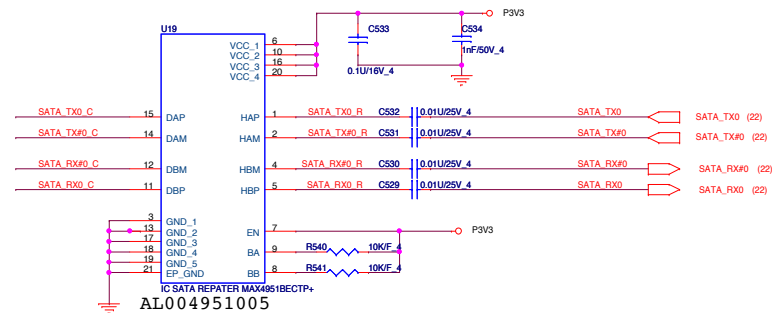
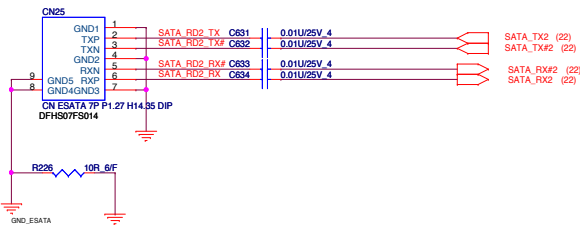
Check New ODD CONN Pin Define.

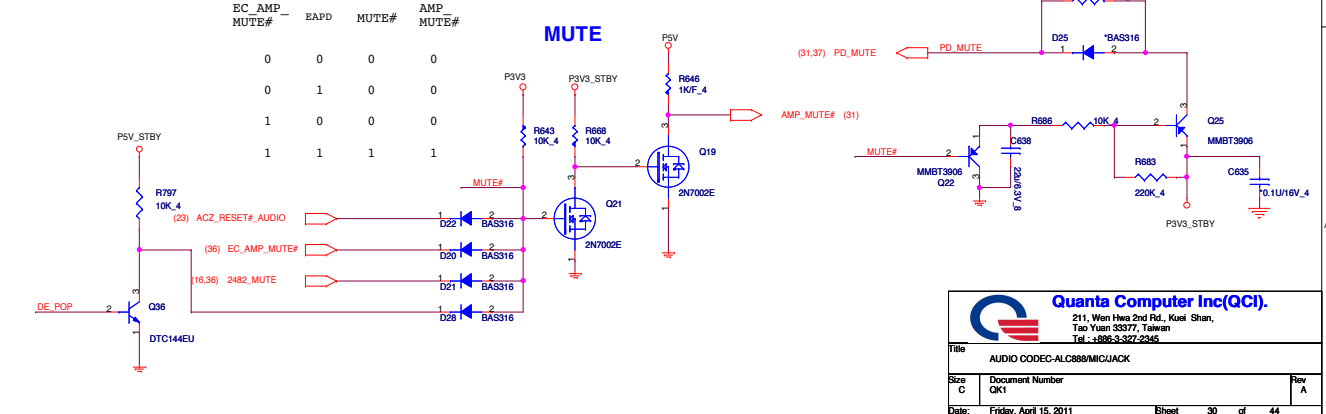
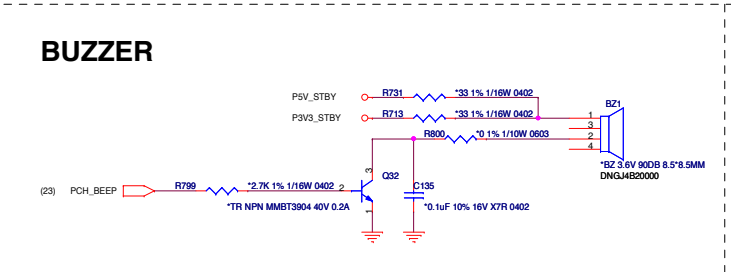
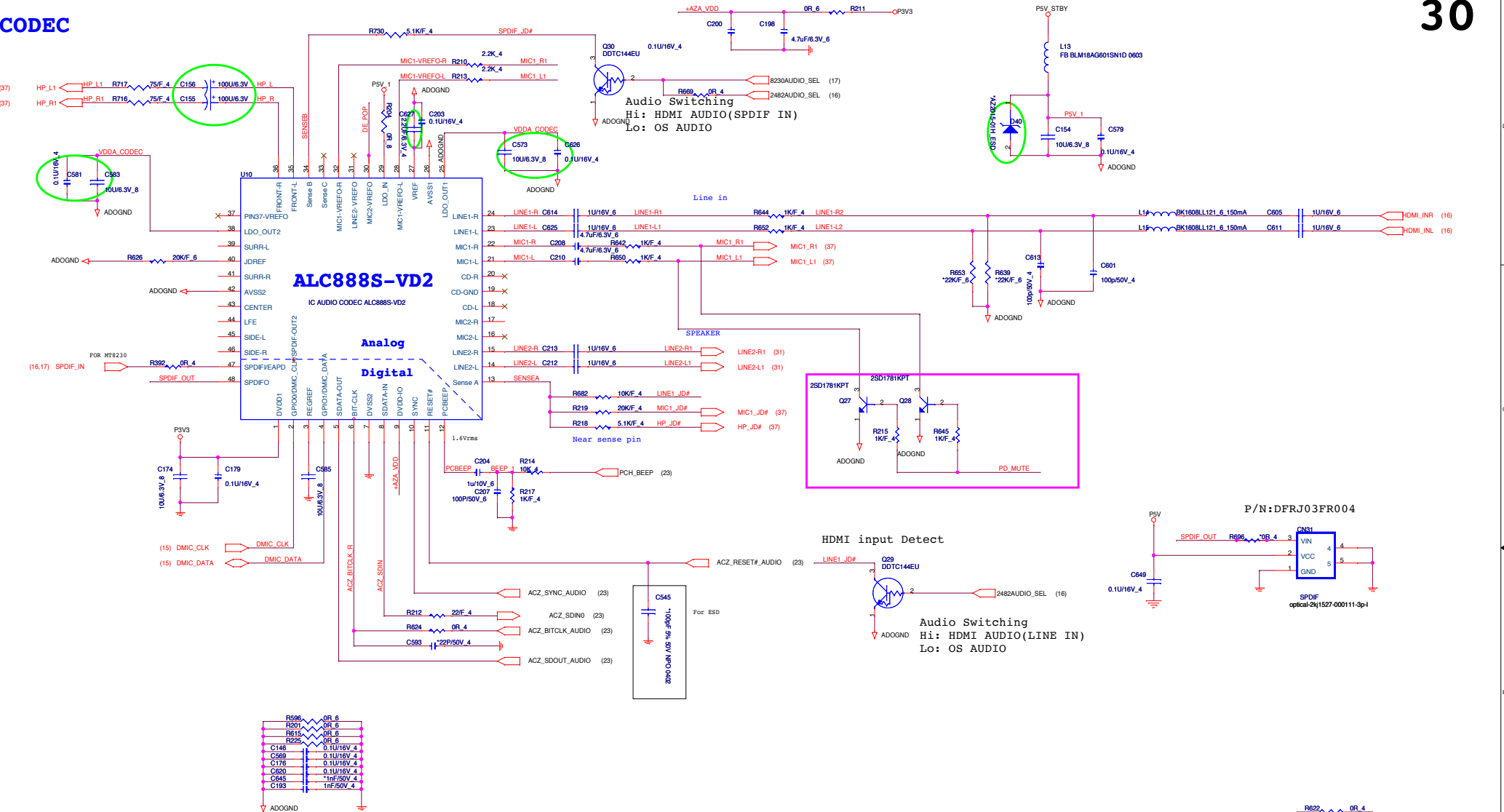


SATA HDD(3.5")

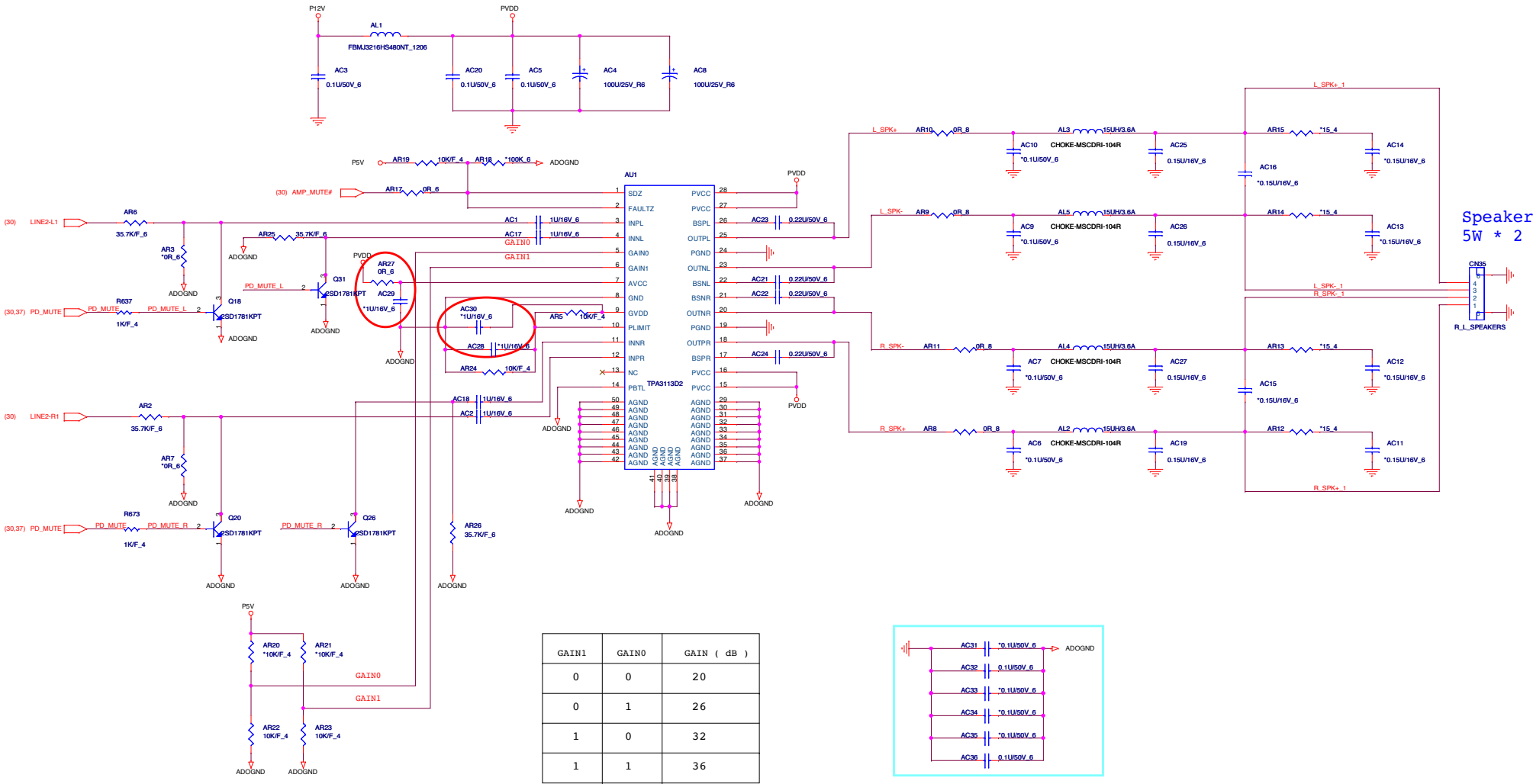


ESATA CONN





Speaker AMP.

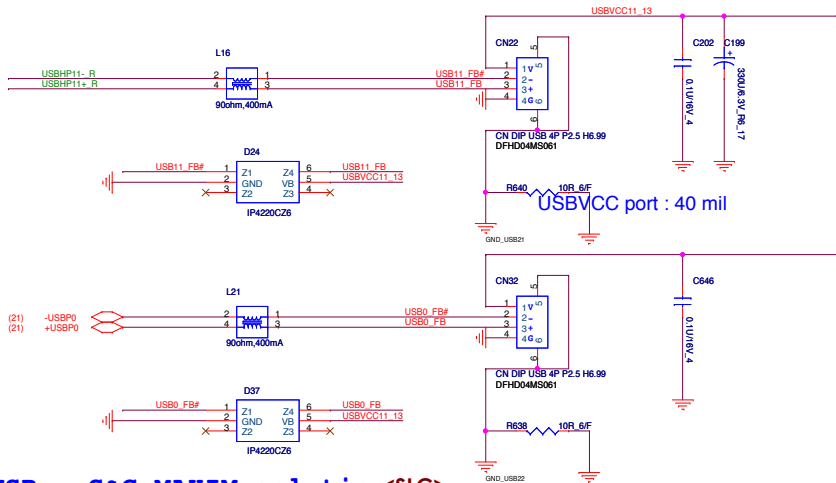


REAR USB PORT X4

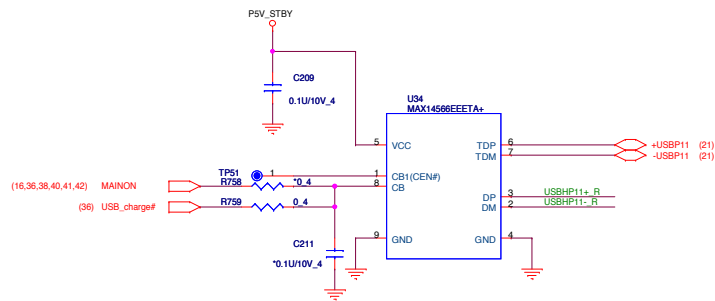
USBVCC port : 40 mil

Touch Panel connector

80 mil



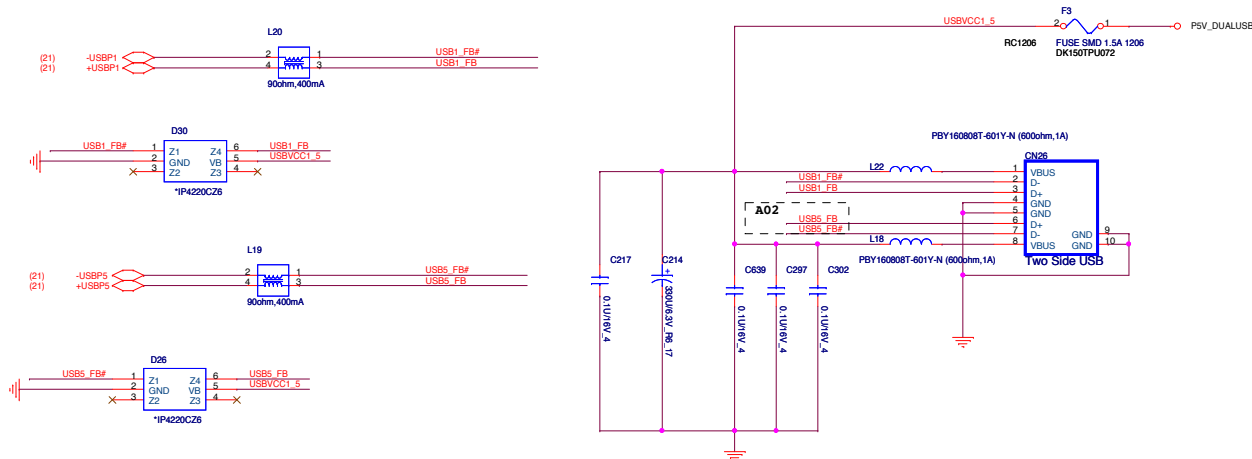
USB w S&C MAXIM solution<SLC>



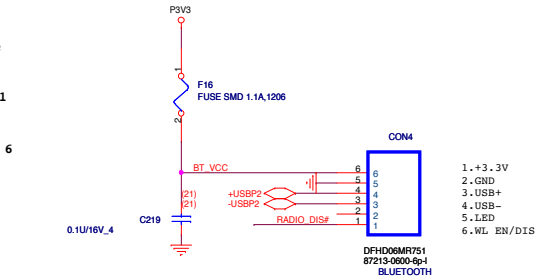
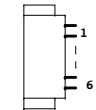
CB0	CB1	Status
0	0	Auto mode
0	1	Force dedicated charger mode
1	X	Pass-Through(USB) mode: Connect DP/DM to TDP/TDM

SIDE USB PORT X2

USBVCC port : 80 mil



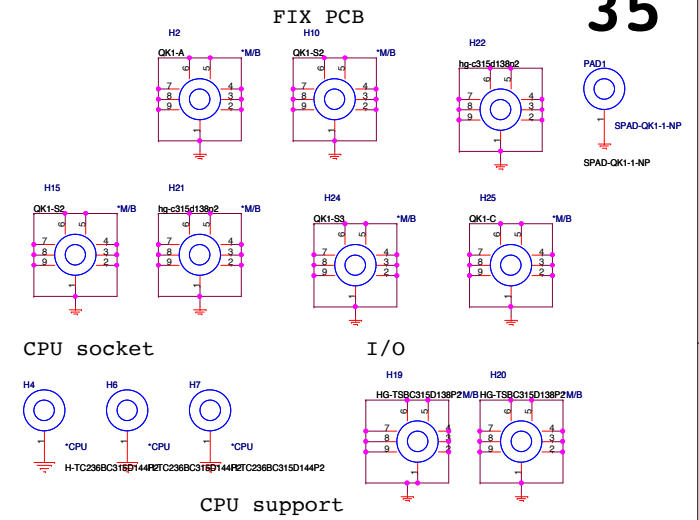
TOP Side



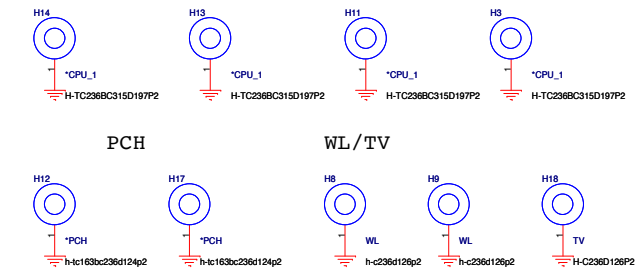
BT Connector

[Activate: H]

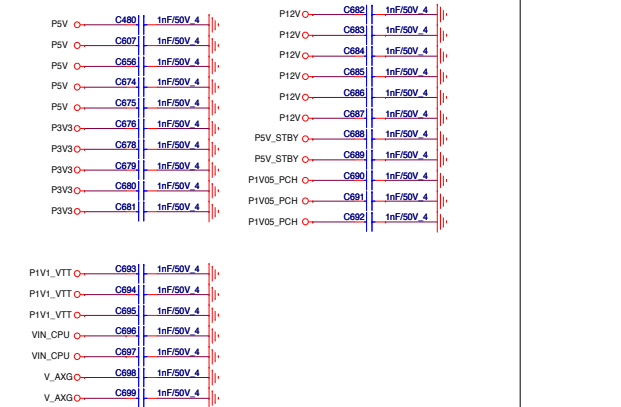
- 1. +3.3V
- 2. GND
- 3. USB+
- 4. USB-
- 5. LED
- 6. WL EN/DIS



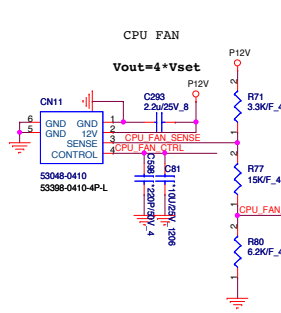
CPU support



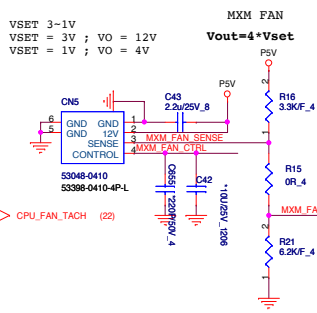
FOR EMI



System FAN CONN



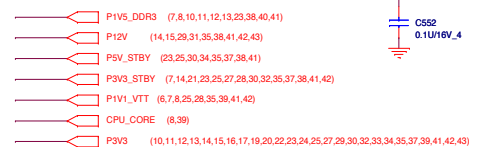
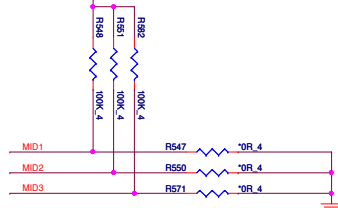
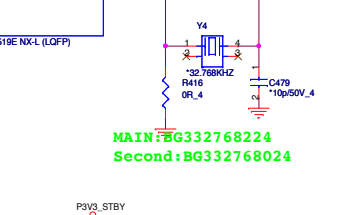
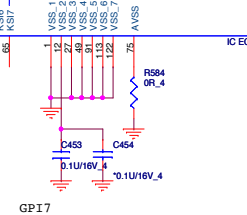
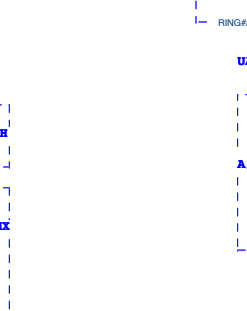
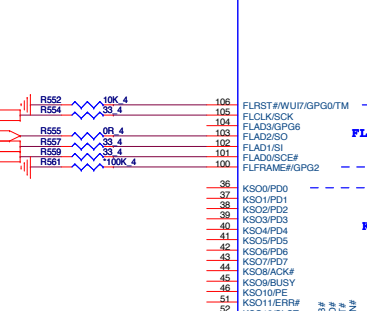
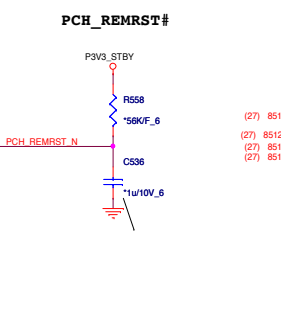
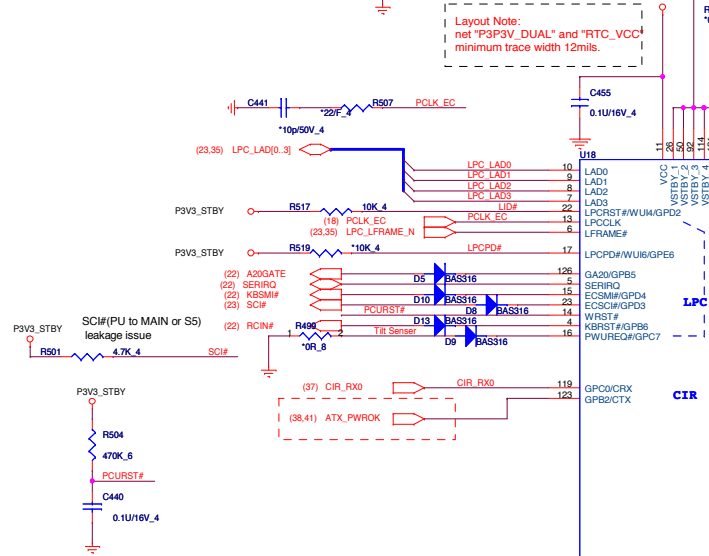
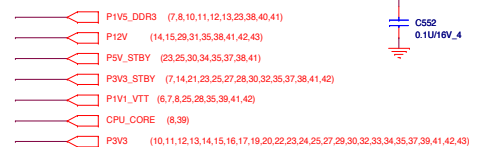
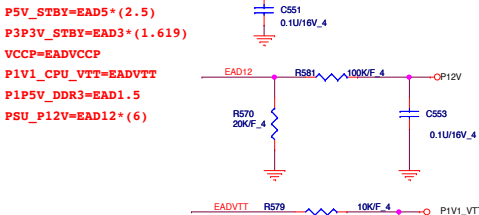
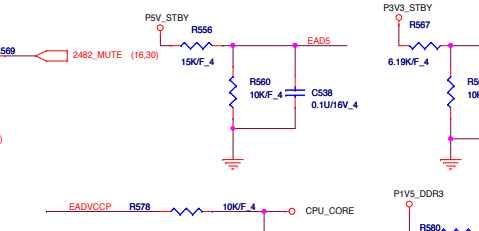
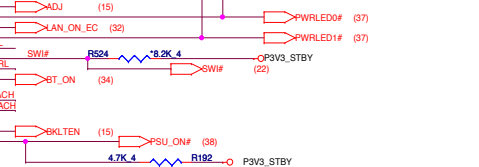
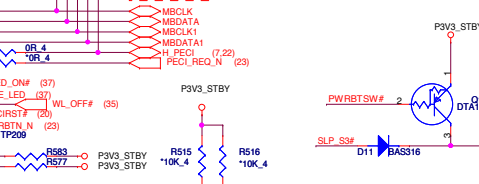
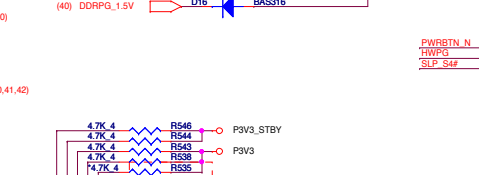
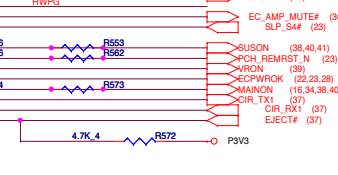
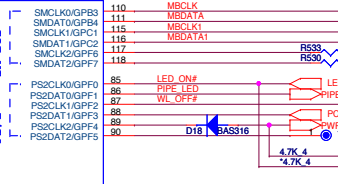
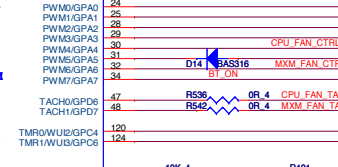
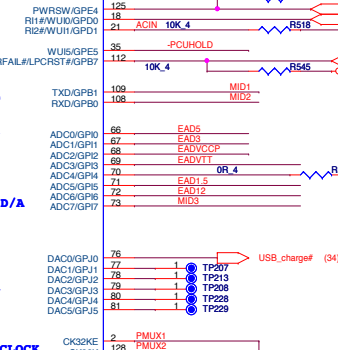
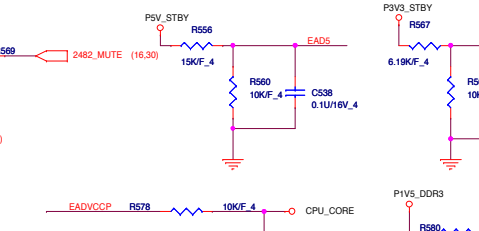
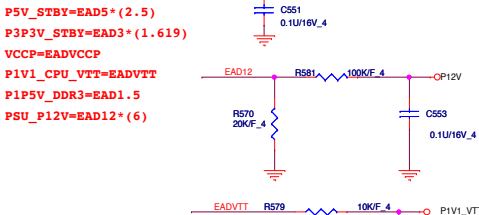
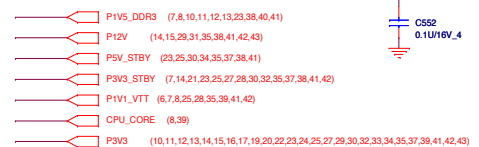
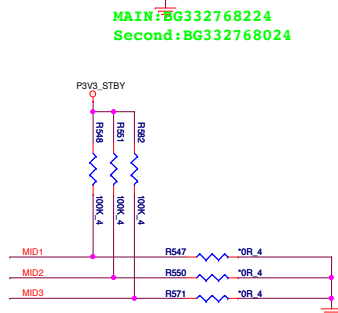
2nd FAN CONN



GPI7	
MID3	
1	OS(default)
0	Free DOS

MID1	MID2	
1	1	ACER(default)
1	0	Gateway
0	1	Packard Bell
0	0	

OFF=1= Hi On= 0= Low



[illegible]

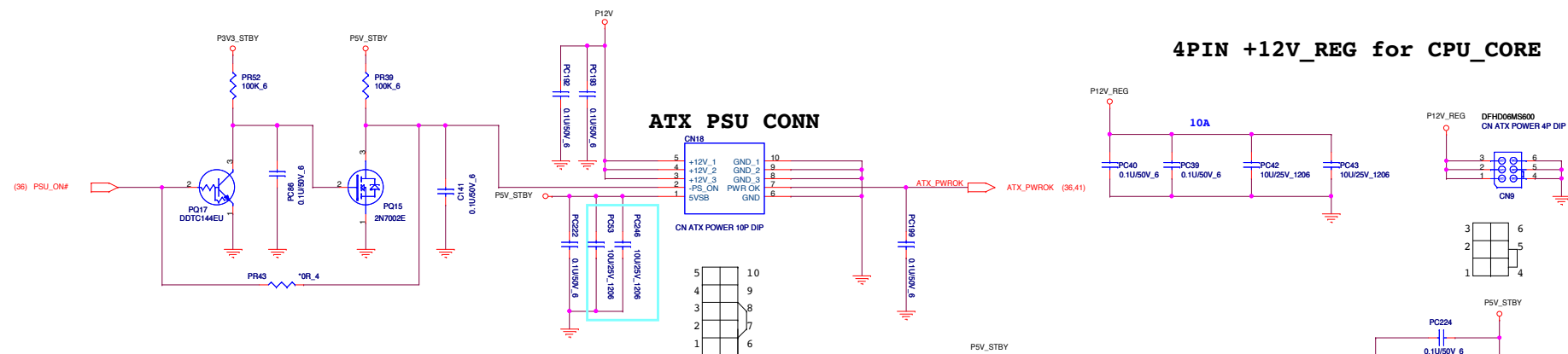
The schematic diagram illustrates the electrical circuit for a Light Bar. Key components and connections include:

- Control Unit (Left):** Features connector **CN36** (85204-0200) with pins 1, 2, 3, and 4. Pin 1 is grounded, pin 2 is connected to the positive terminal of capacitor **C206** (0.1u/16V_4), and pin 3 is connected to the positive terminal of capacitor **C304** (0.1u/16V_4). Pin 4 is connected to the positive terminal of capacitor **C206**.
- Light Bar (Right):** Features connector **CN27** (DFWF02MS118, CN M 2P 1.25mm SMD WHITE) with pins 1, 2, and 3. Pin 1 is grounded, pin 2 is connected to the positive terminal of capacitor **C304**, and pin 3 is connected to the positive terminal of capacitor **C206**.
- Transistors:** **Q4** (TR M-FET-P AO3413 -20V -0.3A) and **Q5** (DTC144EU) are shown. **Q4** is connected to the positive terminal of capacitor **C206** and the positive terminal of capacitor **C304**. **Q5** is connected to the positive terminal of capacitor **C206** and the positive terminal of capacitor **C304**.
- Resistors:** **R206** (100K_6) is connected between the positive terminal of capacitor **C206** and the positive terminal of capacitor **C304**.
- Fuse:** **F15** (FUSE SMD 1.1A, 1206) is connected between the positive terminal of capacitor **C206** and the positive terminal of capacitor **C304**.
- Diode:** **DTC144EU** is connected between the positive terminal of capacitor **C206** and the positive terminal of capacitor **C304**.
- Power Supply:** **PSV_STBY** and **PSV_DUAL** are shown. **PSV_STBY** is connected to the positive terminal of capacitor **C206** and the positive terminal of capacitor **C304**. **PSV_DUAL** is connected to the positive terminal of capacitor **C206** and the positive terminal of capacitor **C304**.

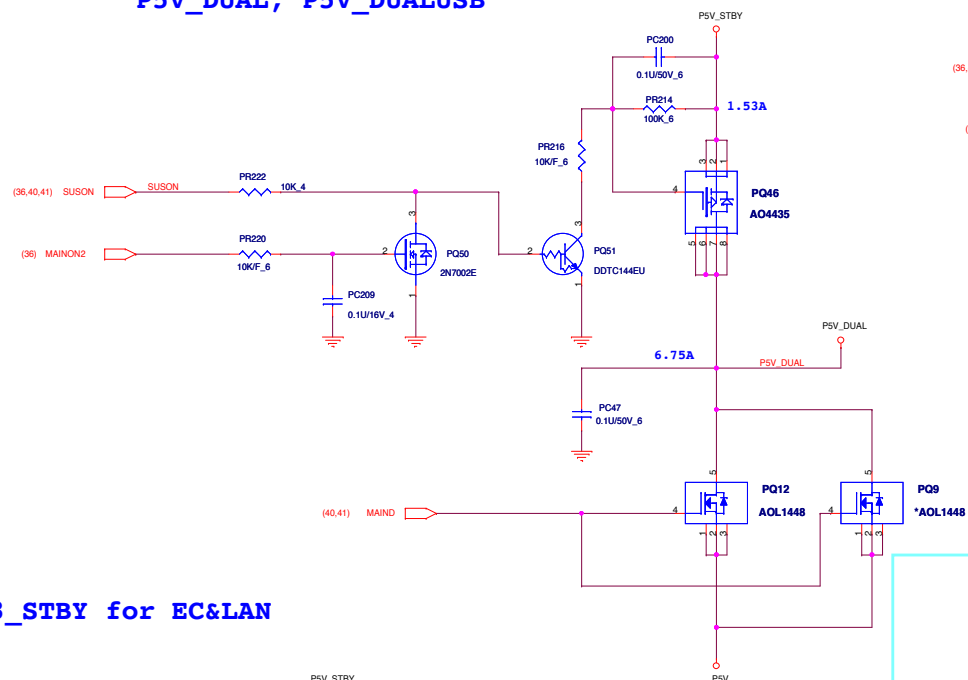
4 CN16
 1
 2
 3
 5
 CN 3P M 1.5mm SMT
 DFWF03MS091
 85205-03XX-3P-L-SMT
 C660
 *220P50V_4
 R754 0R_4
 R776 *0R_4
 EJECT# (36)
 HW_EJECT# ()

[illegible]

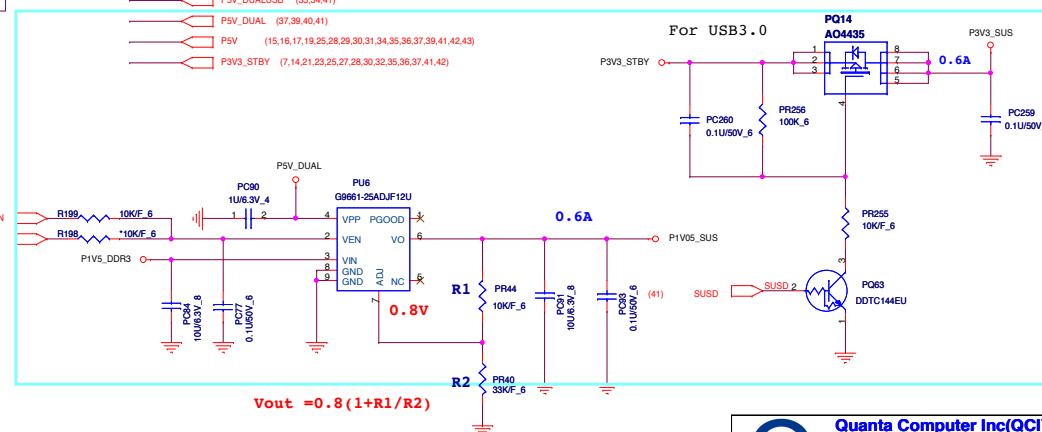
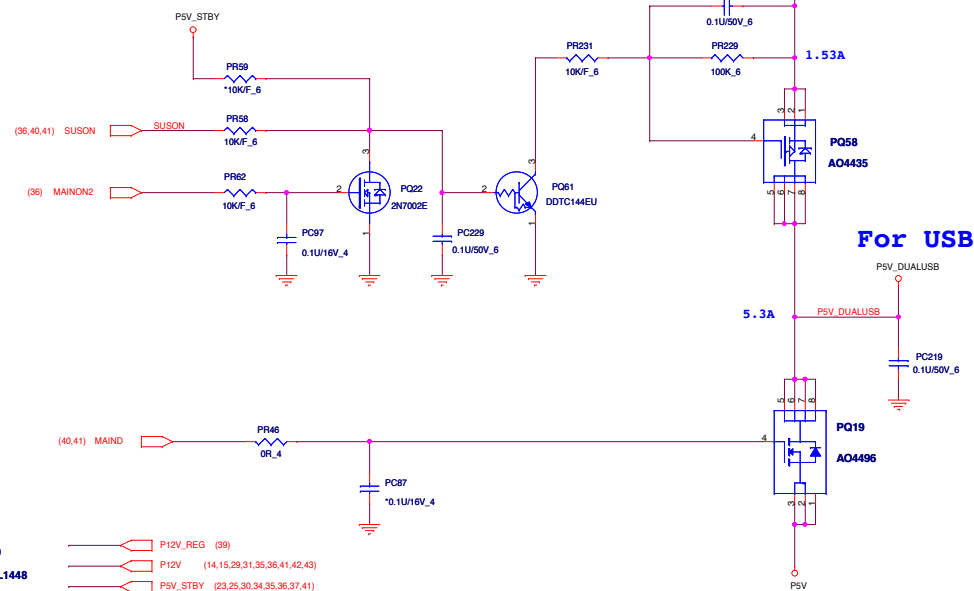
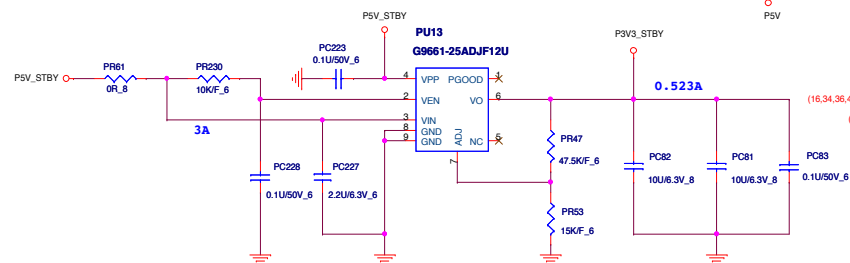
4PIN +12V_REG for CPU_CORE



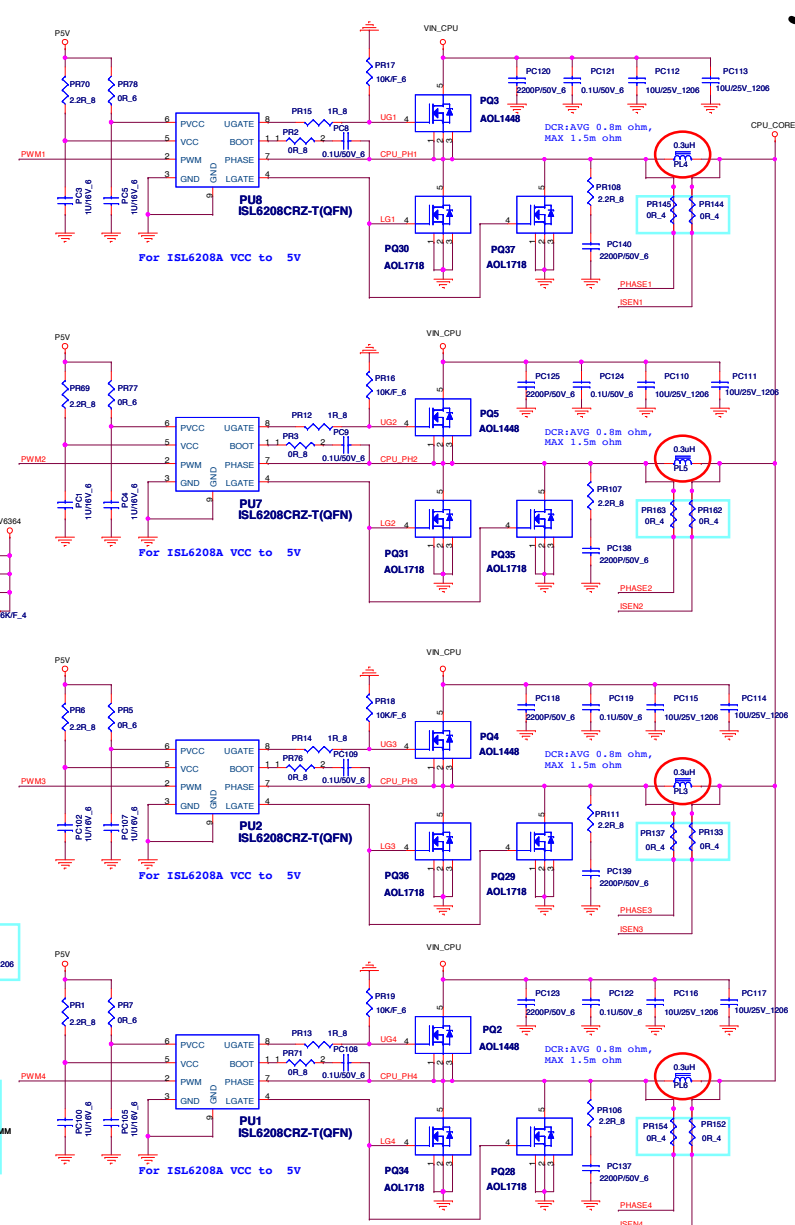
P5V_DUAL, P5V_DUALUSB



P3V3_STBY for EC&LAN



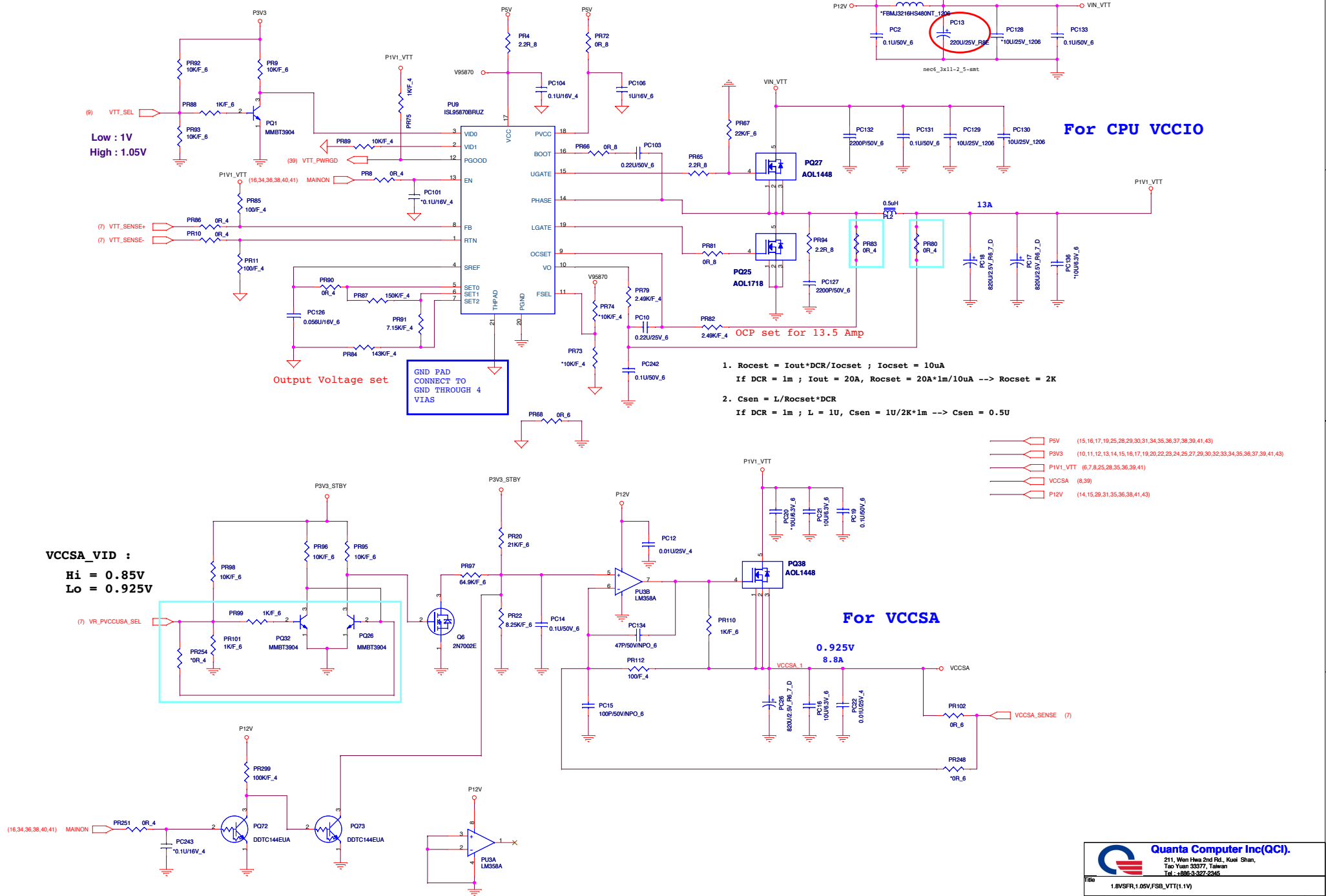
$$V_{out} = 0.8(1 + R1/R2)$$



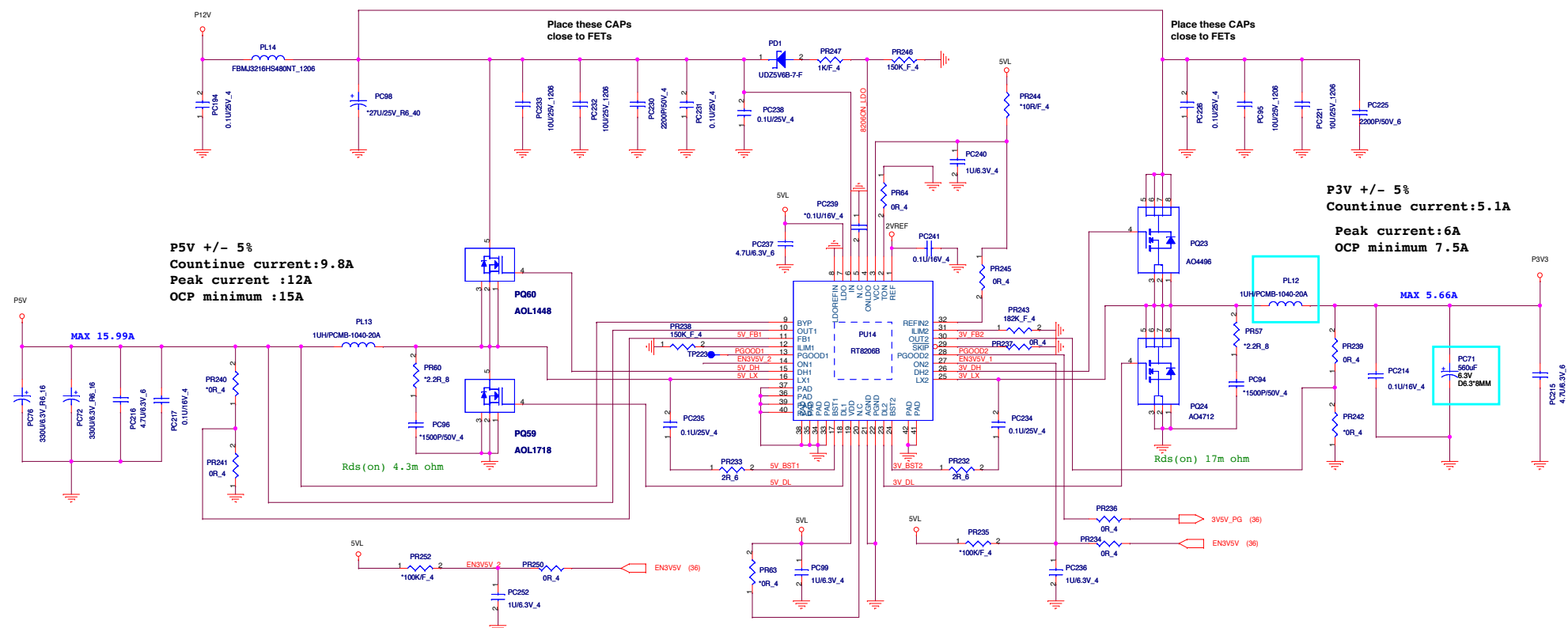
- | | |
|---------------|---|
| P12V | (14,15,29,31,35,36,38,41,42,43) |
| P12V_REG (3#) | |
| PSV_DUAL | (37,38,40,41) |
| PSV | (15,16,17,19,25,29,29,30,31,34,35,36,37,38,41,42,43) |
| PSV3 | (10,11,12,13,14,15,16,17,19,20,22,23,24,25,27,29,30,32,33,34,35,36,37,41,42,43) |
| P1V1_VTT | (6,7,8,25,28,35,36,41,42) |
| VCCSA | (8,42) |
| CPU_CORE | (8,36) |
| V_AXG | (8,35) |

ISL95870B For VTT

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SYSTEM POWER P3V3 / P5V



$$I_{ocp} = (V_{trip} / R_{ds_on}) + (I_{ripple} / 2) = (V_{trip}/R_{ds_on}) + (1/(2 * L * f) * (V_{in} - V_{out}) * V_{out} / V_{in})$$

A01718 MOSFET $R_{ds_on} = 3.4 \text{ m ohm} \sim 4.3 \text{ m ohm}$

5VPCU Operate Freqeunce by 400kHz

$R_{trip} = 150 \text{ K ohm}$

$V_{trip} = 150 \text{ K ohm} * 5/10 = 75 \text{ mV}$

$PL12 = 3.3 \text{ uH}$

$I_{ocp_5VPCU} = 17.4 \sim 22 \text{ A}$

3VPCU Operate Freqeunce by 500kHz

$R_{trip} = 182 \text{ K ohm}$

$V_{trip} = 182 \text{ K ohm} * 5/10 = 91 \text{ mV}$

$PL8 = 4.7 \text{ uH}$ $I_{ocp_3VPCU} = 6.06 \sim 5.05 \text{ A}$

P12V (14,15,29,31,35,36,38,41,42)
 P5V (15,16,17,19,25,26,29,30,31,34,35,36,37,38,39,41,42)
 P3V3 (10,11,12,13,14,15,16,17,19,20,22,23,24,25,27,29,30,32,33,34,35,36,37,39,41,42)

PCB REV:B

2010/07/22:
P31 Remove Buzzer circuit
P15 Nexchange B_EXP_RX_N1 and NB_EXP_RX_P1
2010/07/23:
P39, PR225 change to 10K
P35, Remove 3D RF circuit
P38, ADD left pipe LED circuit, Change CN38 for Light and home button control
P30, Remove CN11 SSD power CONN
2010/07/27
P24 ADD R714, ADD R713 Pull up H_SKTOCC_N
P30. CN19 inverse 180 degree
2010/07/28
P4 Remove CLOCK GEN circuit
P42 Remove PU6, PR51
P24 DEL Q4,Q5
P28 Remove Q7

PCB REV:D

2010/10/21:
P19, Add Q34,Q35,R732,R733,R752,R753 for DP ctrl level shift
P34, Add U34,C209,C211,R758,R759 for usb charge
2010/11/03:
P37,CON5 modify pin define.
2010/11/04
P37,CN27,CN36 Pin1,2 exchange
2010/11/05:
P37,Add R754,R776,R777 for odd eject
P34,Add CN42 for touch power
2010/11/17:
P16,Add CN21 for DVI EDID Flash
P33,Add R778,R779,R780,R787 for USB 3.0
P37,Del R216,R708,C648,Q26
2010/11/22
1.P15 CN1 change CONN for EMI issue
2010/11/23
1.DelR247,R248,R674,R655,R710,R712,R697,R698,R692,R693 for EMI
2.Add RN1~RN7 for EMI
3.P16,Del con2,add CN43 for EMI
2010/11/24
1.P30,Add Q36,D28 for AUDIO
2.P31,Add Q26,Q31 for Audio mute
2010/11/26
1.Add PD2 for CIR
2.Add R247、R248、R405、R654、R672、R674、R687、R688、R693、R697、R698、R703 for EMI

Power portion

- 1. Page 31. Audio Power source PVDD output circuit
- 2. Page 38. Change PSU connector to 6pin and 10 pin, add component location PC53, PC249 for 5VSTBY source
- 3. Page 40. Change PU12 pin17 connect line to GND, change location PL9 footprint
- 4. Page 40. Change PU12 pin17 connect line to GND, change location PL9 footprint

PCB REV:E

- 1. Page 30. Q36 change type from 2n7002 to DTC144EU for audio
- 2010/12/16
- 1. Page 28. Add R351,R711,R712
- 2010/12/28
- 1. Page 30. Add BZ1 (reserve Buzzer)

- 2011/01/24
- 1. Page 15. Del R234,R239 Add F7,F8 for safety
 - 2. Page 34. Del R177, Add F9,F10,F16 for safety
 - 3. Page 35. Add F11 for safety
 - 4. Page 37. Del R638,R216, Add F12,F13,F15,F17 for safety
 - 5. Page 34. Add C297,C302 for EMI

PCB REV:F

- 1. Page 17. Del D31,D43 add R801,R802 for HDMI Sink
- 2. Page 23. C108, C109 change to 15pF
- 3. Page 38. PQ14 change type from SI4116DY to AO4435 for USB30
- 4. Page 38. Remove R628、R634、add L25 for EMI

Title			
Change List			
Size	Document Number		Rev
C	QK1		<Rev Code>
Date:	Friday, April 29, 2011	Sheet	44 of 44